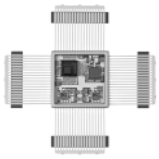


ENHANCED MINIATURE ADVANCED COMMUNICATIONS ENGINE (ENHANCED MINI-ACE)

DESCRIPTION

The Enhanced Mini-ACE family of MIL-STD-1553 terminals provide complete interfaces between a host processor and a 1553 bus. These terminals integrate dual transceiver, protocol logic, and 4K words or 64K words of RAM.

With a 1.0 inch square package, the Enhanced Mini-ACE is nearly 100% footprint and software compatibile with the previous generation Mini-ACE (Plus) terminals, and is software compatibile with the older ACE series.

The Enhanced Mini-ACE is powered by a choice 5V, or 5V/3.3V (3.3V logic). Multiprotocol support of MIL-STD-1553A/B and STANAG 3838, including versions incorporating McAir compatible transmitters, is provided. There is a choice of 10, 12, 16, or 20 Mhz clocks. The BC/RT/MT versions with 64K words of RAM include built-in RAM parity checking.

BC features include a built-in message sequence control engine, with a set of 20 instructions. This provides an autonomous means of implementing multi-frame message scheduling, message retry schemes, data double buffering, asynchronous message insertion, and reporting to the host CPU. The Enhanced Mini-ACE incorporates a fully autonomous built-in self-test, which provides comprehensive testing of the internal protocol logic and/or RAM.

The Enhanced Mini-ACE RT offers the same choices of subaddress buffering as the ACE and Mini-ACE (Plus), along with a global circular buffering option, 50% rollover interrupt for circular buffers, an interrupt status queue, and an "Auto-boot" option to support MIL-STD-1760.

The Enhanced Mini-ACE terminals provide the same flexibility in host interface configurations as the ACE/Mini-ACE, along with a reduction in the host processor's worst case holdoff time.

FEATURES

- *FULLY INTEGRATED 1553A/B NOTICE 2, MCAIR, STANAG 3838 INTERFACE TERMINAL*
- *COMPATIBLE WITH MINI-ACE (PLUS) AND ACE GENERATIONS*
- *CHOICE OF :*
  - *RT OR BC/RT/MT IN SAME FOOTPRINT*
  - *RT OR BC/RT/MT WITH 4K RAM*
  - *BC/RT/MT WITH 64K RAM, WITH RAM PARITY*
- *CHOICE OF 5V OR 3.3V LOGIC*
- *5V TRANSCEIVER WITH 1760 AND MCAIR COMPATIBLE OPTIONS*
- *COMPREHENSIVE BUILT-IN SELF-TEST*
- *FLEXIBLE PROCESSOR/MEMORY INTERFACE, WITH REDUCED HOST WAIT TIME*
- *CHOICE OF 10, 12, 16, OR 20 MHZ CLOCK*
- *HIGHLY AUTONOMOUS BC WITH BUILT-IN MESSAGE SEQUENCE CONTROL:*
  - *FRAME SCHEDULING*
  - *BRANCHING*
  - *ASYNCHRONOUS MESSAGE INSERTION*
  - *GENEERAL PURPOSE QUEUE*
  - *USER-DEFINED INTERRUPTS*
- *ADVANCED RT FUNCTIONS*
  - *GLOBAL CIRCULAR BUFFERING*
  - *INTERRUPT STATUS QUEUE*
  - *50% CIRCULAR BUFFER ROLLOVER INTERRPTS*

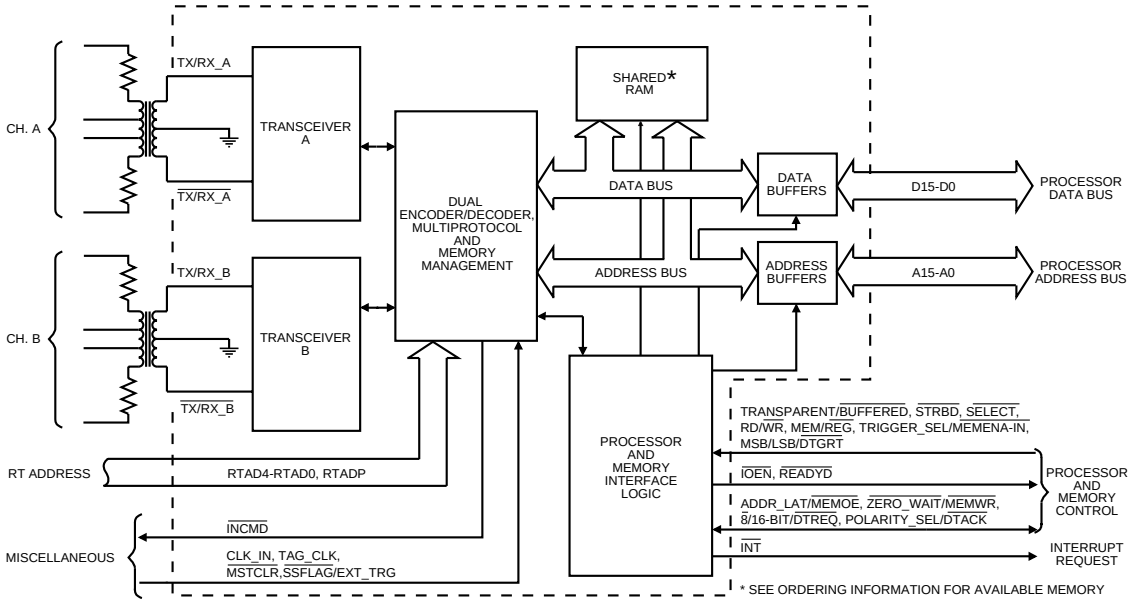


FIGURE 1. ENHANCED MINI-ACE BLOCK DIAGRAM

TABLE 1. EHANCED MINI-ACE SERIES SPECIFICATIONS				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
ABSOLUTE MAXIMUM RATING				
Supply Voltage				
■ Logic +5V or +3.3V	-0.3		6.0	V
■ RAM +5V	-0.3		6.0	V
■ Transceiver +5V (Note 11)	-0.3		7.0	V
Logic				
■ Voltage Input Range for +5V Logic (BU-61XX5)	-0.3		6.0	V
■ Voltage Input Range for +3.3V Logic (BU-61XX3/4)	-0.3		6.0	V
RECEIVER				
Differential Input Resistance (Notes 1-6)	2.5			kΩ
Differential Input Capacitance (Notes 1-6)			5	pF
Threshold Voltage, Transformer Coupled, Measured on Stub	0.200		0.860	Vp-p
Common Mode Voltage (Note 7)			10	Vpeak
TRANSMITTER				
Differential Output Voltage				
■ Direct Coupled Across 35 Ω, Measured on Bus	6	7	9	Vp-p
■ Transformer Coupled Across 70 Ω, Measured on Bus				
(BU-61XXXXX-XX0,	18	20	27	Vp-p
BU-61XXXXX-XX2) (Note 13)	20	22	27	Vp-p
Output Noise, Differential (Direct Coupled)			10	mV_{P-P}
Output Offset Voltage, Transformer Coupled Across 70 ohms	-250		250	mV_{peak}
Rise/Fall Time				
(BU-61XXXX3,	100	150	300	nsec
BU-61XXXX4)	200	250	300	nsec
LOGIC				
V_{IH}				
All signals except CLK_IN	2.1			V
CLK_IN	0.8•Vcc			V
V_{IL}				
All signals except CLK_IN			0.7	V
CLK_IN			0.2•Vcc	V
Schmidt Hysteresis				
All signals except CLK_IN	0.4			V
CLK_IN	1.0			V
I_{IH}, I_{IL}				
All signals except CLK_IN				
I_{IH} (Vcc=5.5V, V_{IN}=Vcc)	-10		10	µA
I_{IH} (Vcc=5.5V, V_{IN}=2.7V)	-350		-50	µA
I_{IL} (Vcc=3.6V, V_{IN}=Vcc)	-10		10	µA
I_{IH} (Vcc=3.6V, V_{IH}=2.7V)	-350		-33	µA
I_{IL} (Vcc=5.5V, V_{IH}=0.4V)	-350		-50	µA
I_{IL} (Vcc=3.6V, V_{IH}=0.4V)	-350		-33	µA
CLK_IN				
I_{IH}	-10		10	µA
I_{IL}	-10		10	µA
V_{OH} (Vcc=4.5V, V_{IH}=2.7V, V_{IL}=0.2V, I_{OH}=max)	2.4			V
V_{OH} (Vcc=3.0V, V_{IH}=2.7V, V_{IL}=0.2V, I_{OH}=max)	2.4			V
V_{OL} (Vcc=4.5V, V_{IH}=2.7V, V_{IL}=0.2V, I_{OL}=max)			0.4	V
V_{OL} (Vcc=3.0V, V_{IH}=2.7V, V_{IL}=0.2V, I_{OL}=max)			0.4	V
I_{OL}	3.4			mA
I_{OH}			-3.4	mA
C_I (Input Capacitance)			50	pF
C_{IO} (Bi-directional signal input capacitance)			50	pF

TABLE 1. EHANCED MINI-ACE SERIES SPECIFICATIONS (Cont'd)				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
POWER SUPPLY REQUIREMENTS				
Voltages/Tolerances				
■ +5V (RAM for 61864(5), Logic for BU-61XX5) (Note 11)	4.5	5.0	5.5	V
■ +3.3V (Logic for BU-61XX3/4) (Note 11)	3.0	3.3	3.6	V
■ +5V (Ch. A, Ch. B)	4.75	5.0	5.5	V
Current Drain (Total Hybrid)				
■ BU-61865XX-XX0				
+5V (Logic, RAM, Ch. A, Ch. B)				
• Idle			180	mA
• 25% Transmitter Duty Cycle			285	mA
• 50% Transmitter Duty Cycle			390	mA
• 100% Transmitter Duty Cycle			600	mA
■ BU-61865X3-XX2				
+5V (Logic, RAM, Ch. A, Ch. B)				
• Idle			180	mA
• 25% Transmitter Duty Cycle			296	mA
• 50% Transmitter Duty Cycle			412	mA
• 100% Transmitter Duty Cycle			645	mA
■ BU-61864XX-XX0				
+5V (RAM, Ch. A, Ch. B)				
• Idle			120	mA
• 25% Transmitter Duty Cycle			225	mA
• 50% Transmitter Duty Cycle			330	mA
• 100% Transmitter Duty Cycle			540	mA
• 3.3V Logic			40	mA
■ BU-61864X3-XX2				
+5V (RAM, Ch. A, Ch. B)				
• Idle			120	mA
• 25% Transmitter Duty Cycle			236	mA
• 50% Transmitter Duty Cycle			352	mA
• 100% Transmitter Duty Cycle			585	mA
• 3.3V Logic			40	mA
■ BU-61745XX-XX0. BU-61845XX-XX0				
+5V (Logic, RAM, Ch. A, Ch. B)				
• Idle			160	mA
• 25% Transmitter Duty Cycle			265	mA
• 50% Transmitter Duty Cycle			370	mA
• 100% Transmitter Duty Cycle			580	mA
■ BU-61745X3-XX2. BU-61845X3-XX2				
+5V (Logic, RAM, Ch. A, Ch. B)				
• Idle			160	mA
• 25% Transmitter Duty Cycle			276	mA
• 50% Transmitter Duty Cycle			392	mA
• 100% Transmitter Duty Cycle			625	mA
■ BU-61743XX-XX0, BU-61843XX-XX0				
+5V (Ch. A, Ch. B)				
• Idle			100	mA
• 25% Transmitter Duty Cycle			205	mA
• 50% Transmitter Duty Cycle			310	mA
• 100% Transmitter Duty Cycle			520	mA
• 3.3V Logic			40	mA
■ BU-61743X3-XX2, BU-61843X3-XX2				mA
+5V (Ch. A, Ch. B)				
• Idle			100	mA
• 25% Transmitter Duty Cycle			216	mA
• 50% Transmitter Duty Cycle			332	mA
• 100% Transmitter Duty Cycle			565	mA
• 3.3V Logic			40	mA

TABLE 1. EHANCED MINI-ACE SERIES SPECIFICATIONS (Cont'd)				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
POWER DISSIPATION (Note 14)				
Total Hybrid				
■ BU-61865XX-XX0				
• Idle			0.99	W
• 25% Transmitter Duty Cycle			1.22	W
• 50% Transmitter Duty Cycle			1.45	W
• 100% Transmitter Duty Cycle			1.90	W
■ BU-61865X3-XX2				
• Idle			0.99	W
• 25% Transmitter Duty Cycle			1.28	W
• 50% Transmitter Duty Cycle			1.58	W
• 100% Transmitter Duty Cycle			2.16	W
■ BU-61864XX-XX0				
• Idle			0.80	W
• 25% Transmitter Duty Cycle			1.03	W
• 50% Transmitter Duty Cycle			1.26	W
• 100% Transmitter Duty Cycle			1.71	W
■ BU-61864X3-XX2				
• Idle			0.80	W
• 25% Transmitter Duty Cycle			1.09	W
• 50% Transmitter Duty Cycle			1.39	W
• 100% Transmitter Duty Cycle			1.97	W
■ BU-61745XX-XX0, BU-61845XX-XX0				
• Idle			0.88	W
• 25% Transmitter Duty Cycle			1.11	W
• 50% Transmitter Duty Cycle			1.33	W
• 100% Transmitter Duty Cycle			1.79	W
■ BU-61745X3-XX2, BU-61845X3-XX2				
• Idle			0.88	W
• 25% Transmitter Duty Cycle			1.17	W
• 50% Transmitter Duty Cycle			1.46	W
• 100% Transmitter Duty Cycle			2.05	W
■ BU-61743XX-XX0, BU-61843XX-XX0				
• Idle			0.69	W
• 25% Transmitter Duty Cycle			0.92	W
• 50% Transmitter Duty Cycle			1.15	W
• 100% Transmitter Duty Cycle			1.60	W
■ BU-61743X3-XX2, BU-61843X3-XX2				
• Idle			0.69	
• 25% Transmitter Duty Cycle			0.98	W
• 50% Transmitter Duty Cycle			1.28	W
• 100% Transmitter Duty Cycle			1.86	W
Hottest Die				W
■ BU-61XXXXX-XX0				
• Idle			0.28	W
• 25% Transmitter Duty Cycle			0.51	W
• 50% Transmitter Duty Cycle			0.75	W
• 100% Transmitter Duty Cycle			1.22	W
■ BU-61XXXX3-XX2				
• Idle			0.28	W
• 25% Transmitter Duty Cycle			0.58	W
• 50% Transmitter Duty Cycle			0.88	W
• 100% Transmitter Duty Cycle			1.48	W

TABLE 1. EHANCED MINI-ACE SERIES SPECIFICATIONS (Cont'd)				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
CLOCK INPUT				
Frequency				
■ Nominal Value				
• Default Mode		16.0		MHz
• Option		12.0		MHz
• Option		10.0		MHz
• Option		20.0		MHz
■ Long Term Tolerance				
• 1553A Compliance	-0.01		0.01	%
• 1553B Compliance	-0.10		0.1	%
■ Short Term Tolerance, 1 second				
• 1553A Compliance	0.001		0.001	%
• 1553B Compliance	-0.01		0.01	%
■ Duty Cycle	40		60	%
1553 MESSAGE TIMING				
Completion of CPU Write (BC Start)-to-Start of Next Message for (Non-enhanced BC Mode)		2.5		µs
BC Intermessage Gap (Note 8)				
Non-enhanced (Mini-ACE compatible) BC mode		9.5		µs
Enhanced BC mode (Note 9)		10.0 to 10.5		µs
BC/RT/MT Response Timeout (Note 10)				
■ 18.5 nominal	17.5	18.5	19.5	µs
■ 22.5 nominal	21.5	22.5	23.5	µs
■ 50.5 nominal	49.5	50.5	51.5	µs
■ 128.0 nominal	127	129.5	131	µs
RT Response Time (mid-parity to mid-sync) (Note 11)	4		7	µs
Transmitter Watchdog Timeout		660.5		µs
THERMAL				
Thermal Resistance, Junction-to-Case, Hottest Die (θ_{JC})			20	°C/W
Operating Junction Temperature	-55		150	°C
Storage Temperature	-65		150	°C
Lead Temperature (soldering, 10 sec.)			+300	°C
PHYSICAL CHARACTERISTICS				
Size	1.0 X 1.0 X 0.155 (25.4 x 25.4 x 3.94)			in. (mm)
Weight	0.6 (17)			oz (g)

NOTES:

Notes 1 through 6 are applicable to the Receiver Differential Resistance and Differential Capacitance specifications:

(1) Specifications include both transmitter and receiver (tied together internally).

(2) Impedance parameters are specified directly between pins TX/RX A(B) and $\overline{\text{TX/RX A(B)}}$ of the Enhanced Mini-ACE hybrid.

(3) It is assumed that all power and ground inputs to the hybrid are connected.

(4) The specifications are applicable for both unpowered and powered conditions.

(5) The specifications assume a 2 volt rms balanced, differential, sinusoidal input. The applicable frequency range is 75 kHz to 1 MHz.

(6) Minimum resistance and maximum capacitance parameters are guaranteed over the operating range, but are not tested.

(7) Assumes a common mode voltage within the frequency range of dc to 2 MHz, applied to pins of the isolation transformer on the stub side (either direct or transformer coupled), and referenced to hybrid ground. Transformer must be a DDC recommended transformer or other transformer that provides an equivalent minimum CMRR.

(8) Typical value for minimum intermessage gap time. Under software control, this may be lengthened to 65,535 ms - message time, in increments of 1 µs. If ENHANCED CPU ACCESS, bit 14 of Configuration Register #6, is set to logic "1", then host accesses during BC Start-of-Message (SOM) and End-of-Message (EOM) transfer sequences could have the effect of lengthening the intermessage gap time. For each host access during an SOM or EOM sequence, the intermessage gap time will be lengthened by 6 clock cycles. Since there are 7 internal transfers during SOM, and 5 during EOM, this could theoretically lengthen the intermessage gap by up to 72 clock cycles; i.e., up to 7.2 ms with a 10 MHz clock, 6.0 µs with a 12 MHz clock, 4.5 µs with a 16 MHz clock, or 3.6 µs with a 20 MHz clock.

(9) For Enhanced BC mode, the typical value for intermessage gap time is approximately 10 clock cycles longer than for the non-enhanced BC mode. That is, an addition of 1.0 µs at 10 MHz, 833 ns at 12 MHz, 625 ns at 16 MHz, or 500 ns at 20 MHz.

(10) Software programmable (4 options). Includes RT-to-RT Timeout (measured mid-parity of transmit Command Word to mid-sync of transmitting RT Status Word).

(11) Measured from mid-parity crossing of Command Word to mid-sync crossing of RT's Status Word.

(12) External 10 µF Tantalum and 0.1 µF capacitors should be located as close as possible to Pins 20 and 72, and a 0.1 µF at pin 37. For BU-61864 and BU-61865, there should also be a 0.1 µF at pin 26.

(13) MIL-STD-1760 requires a 20 Vp-p minimum output on the stub connection.

(14) Power dissipation specifications assume a transformer coupled configuration with external dissipation (while transmitting) of:
0.14 watts for the active isolation transformer,
0.80 watts for the active bus coupling transformer,
0.45 watts for each of the two bus isolation resistors and
0.15 watts for each of the two bus termination resistors.

INTRODUCTION

The BU-61743/61745 RT, and BU-61843/61845/61864/61865 BC/RT/MT Enhanced Mini-ACE family of MIL-STD-1553 terminals comprise a complete integrated interface between a host processor and a MIL-STD-1553 bus. All members of the Enhanced Mini-ACE family are packaged in the same 1.0 square inch flatpack package. The Enhanced Mini-ACE hybrids are nearly 100% footprint and software compatible with the previous generation Mini-ACE and Mini-ACE Plus terminals, and are software compatibility with the original ACE series.

The Enhanced Mini-ACE provides complete multiprotocol support of MIL-STD-1553A/B/McAir and STANAG 3838. All versions integrate dual transceiver; along with protocol, host interface, memory management logic; and a minimum of 4K words of RAM. In addition, the BU-61864 and BU-61865 BC/RT/MT terminals include 64K words of internal RAM, with built-in parity checking.

The Enhanced Mini-ACEs include a 5V, voltage source transceiver for improved line driving capability, with options for MIL-STD-1760 and McAir compatibility. As a means of reducing power consumption, there are versions for which the logic is powered by 3.3V, rather than 5V. To provide further flexibility, the Enhanced Mini-ACE may operate with a choice of 10, 12, 16, or 20 MHz clock inputs.

One of the new salient features of the Enhanced Mini-ACE is its Enhanced bus controller architecture. The Enhanced BC's highly autonomous message sequence control engine provides a means for offloading the host processor for implementing multiframe message scheduling, message retry schemes, data double buffering, and asynchronous message insertion. For the purpose of performing messaging to the host processor, the Enhanced BC mode includes a General Purpose Queue, along with user-defined interrupts.

A second major new feature of the Enhanced Mini-ACE is the incorporation of a fully autonomous built-in self-test. This test provides comprehensive testing of the internal protocol logic. A separate test verifies the operation of the internal RAM. Since the self-tests are fully autonomous, they eliminate the need for the host to write and read stimulus and response vectors.

The Enhanced Mini-ACE RT offers the same choices of single, double, and circular buffering for individual subaddresses as ACE and Mini-ACE (Plus). New enhancements to the RT architecture include a global circular buffering option for multiple (or all) receive subaddresses, a 50% rollover interrupt for circular buffers, an interrupt status queue for logging up to 32 interrupt events, and an option to automatically initialize to RT mode with the Busy bit set. The interrupt status queue and 50% rollover interrupt features are also included as improvements to the Enhanced Mini-ACE's Monitor architecture.

To minimize board space and "glue" logic, the Enhanced Mini-ACE terminals provide the same wide choice of host interface configurations as the ACE and Mini-ACE (Plus). This includes support of interfaces to 16-bit or 8-bit processors, memory or

port type interfaces, and multiplexed or non-multiplexed address/data buses. In addition, with respect to ACE/Mini-ACE (Plus), the worst case processor wait time has been significantly reduced. For example, assuming a 16 MHz clock, this time has been reduced from 2.8 μs to 632 ns for read accesses, and to 570 ns for write accesses.

The Enhanced Mini-ACE series terminals operate over the full military temperature range of -55 to +125°C. Available screened to MIL-PRF-38534C, the terminals are ideal for military and industrial processor-to-1553 applications.

TRANSCEIVERS

The transceivers in the Enhanced Mini-ACE series terminals are fully monolithic, requiring only a +5 volt power input. The transmitters are voltage sources, which provide improved line driving capability over current sources. This serves to improve performance on long buses with many taps. The transmitters also offer an option which satisfies the MIL-STD-1760 requirement for a minimum of 20 volts peak-to-peak, transformer coupled output.

Besides eliminating the demand for an additional power supply, the use of a +5V-only transceiver requires the use of a step-up, rather than a step-down, isolation transformer. This provides the advantage of a higher terminal input impedance than is possible for a 15 volt or 12 volt transmitter. As a result, there is a greater margin for the input impedance test, mandated for the 1553 validation test. This characteristic allows for longer cable lengths between a system connector and the isolation transformers of an embedded 1553 terminal.

To provide compatibility to McAir specs, the Enhanced Mini-ACEs are available with an option for transmitters with increased rise and fall times.

Additionally, for MIL-STD-1760 applications, the Enhanced Mini-ACE provides an option for a minimum stub voltage level of 20 volts peak-to-peak, transformer coupled.

The receiver sections of the Enhanced Mini-ACE are fully compliant with MIL-STD-1553B Notice 2 in terms of front end overvoltage protection, threshold, common mode rejection, and word error rate.

REGISTER AND MEMORY ADDRESSING

The software interface of the Enhanced Mini-ACE to the host processor consists of 24 internal operational registers for normal operation, an additional 24 test registers, plus 64K words of shared memory address space. The Enhanced Mini-ACE's 4K X 16 or 64K X 17 internal RAM resides in this address space.

For normal operation, the host processor only needs to access the lower 32 register address locations (00-1F). The next 32 locations (20-3F) should be reserved, since many of these are used for factory test.

INTERNAL REGISTERS

The address mapping for the Enhanced Mini-ACE registers is illustrated in TABLE 2:

TABLE 2. ADDRESS MAPPING

ADDRESS LINES					REGISTER DESCRIPTION/ACCESSIBILITY
A4	A3	A2	A1	A0	
0	0	0	0	0	Interrupt Mask Register #1 (RD/WR)
0	0	0	0	1	Configuration Register #1 (RD/WR)
0	0	0	1	0	Configuration Register #2 (RD/WR)
0	0	0	1	1	Start/Reset Register (WR)
0	0	0	1	1	Non-Enhanced BC/RT Command Stack Pointer / Enhanced BC Instruction List Pointer Register (RD)
0	0	1	0	0	BC Control Word / RT Subaddress Control Word Register (RD/WR)
0	0	1	0	1	Time Tag Register (RD/WR)
0	0	1	1	0	Interrupt Status Register #1 (RD)
0	0	1	1	1	Configuration Register #3 (RD/WR)
0	1	0	0	0	Configuration Register #4 (RD/WR)
0	1	0	0	1	Configuration Register #5 (RD/WR)
0	1	0	1	0	RT / Monitor Data Stack Address Register (RD)
0	1	0	1	1	BC Frame Time Remaining Register (RD)
0	1	1	0	0	BC Time Remaining to Next Message Register (RD)
0	1	1	0	1	Non-Enhanced BC Frame Time / Enhanced BC Initial Instruction Pointer / RT Last Command / MT Trigger Word Register(RD/WR)
0	1	1	1	0	RT Status Word Register (RD)
0	1	1	1	1	RT BIT Word Register (RD)
1	0	0	0	0	Test Mode Register 0
1	0	0	0	1	Test Mode Register 1
1	0	0	1	0	Test Mode Register 2
1	0	0	1	1	Test Mode Register 3
1	0	1	0	0	Test Mode Register 4
1	0	1	0	1	Test Mode Register 5
1	0	1	1	0	Test Mode Register 6
1	0	1	1	1	Test Mode Register 7
1	1	0	0	0	Configuration Register #6 (RD/WR)
1	1	0	0	1	Configuration Register #7 (RD/WR)
1	1	0	1	0	RESERVED
1	1	0	1	1	BC Condition Code Register (RD)
1	1	0	1	1	BC General Purpose Flag Register (WR)
1	1	1	0	0	BIT Test Status Register (RD)
1	1	1	0	1	Interrupt Mask Register #2 (RD/WR)
1	1	1	1	0	Interrupt Status Register #2 (RD)
1	1	1	1	1	BC General Purpose Queue Pointer / RT-MT Interrupt Status Queue Pointer Register (RD/WR)

TABLE 3. INTERRUPT MASK REGISTER #1 (READ/WRITE 00H)	
BIT	**DESCRIPTION**
15(MSB)	RESERVED
14	RAM PARITY ERROR
13	BC/RT TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	HANDSHAKE FAIL
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	BC STATUS SET / RT MODE CODE / MT PATTERN TRIGGER
0(LSB)	END OF MESSAGE

TABLE 4. CONFIGURATION REGISTER #1 (READ/WRITE 01H)				
BIT	**BC FUNCTION (Bits 11-0 Enhanced Mode Only)**	**RT WITHOUT ALTERNATE STATUS**	**RT WITH ALTERNATE STATUS (Enhanced Only)**	**MONITOR FUNCTION (Enhanced mode only bits 12-0)**
15 (MSB)	RT/$\overline{\text{BC-MT}}$ (logic 0)	(logic 1)	(logic 1)	(logic o)
14	MT/$\overline{\text{BC-RT}}$ (logic 0)	(logic 0)	(logic 0)	(logic 1)
13	CURRENT AREA B/A	CURRENT AREA B/$\overline{\text{A}}$	CURRENT AREA A/$\overline{\text{B}}$	CURRENT AREA B/$\overline{\text{A}}$
12	MESSAGE STOP-ON-ERROR	MESSAGE MONITOR ENABLED (MMT)	MESSAGE MONITOR ENABLED	MESSAGE MONITOR ENABLED
11	FRAME STOP-ON-ERROR	$\overline{\text{DYNAMIC BUS CONTROL ACCEPTANCE}}$	S10	TRIGGER WORD ENABLED
10	STATUS SET STOP-ON-MESSAGE	$\overline{\text{BUSY}}$	S09	START-ON-TRIGGER
9	STATUS SET STOP-ON-FRAME	$\overline{\text{SERVICE REQUEST}}$	S08	STOP-ON-TRIGGER
8	FRAME AUTO-REPEAT	$\overline{\text{SUBSYSTEM FLAG}}$	S07	NOT USED
7	EXTERNAL TRIGGER ENABLED	$\overline{\text{RTFLAG}}$ (Enhanced Mode Only)	S06	EXTERNAL TRIGGER ENABLED
6	INTERNAL TRIGGER ENABLED	NOT USED	S05	NOT USED
5	INTERMESSAGE GAP TIMER ENABLED	NOT USED	S04	NOT USED
4	RETRY ENABLED	NOT USED	S03	NOT USED
3	DOUBLED/$\overline{\text{SINGLE}}$ RETRY	NOT USED	S02	NOT USED
2	BC ENABLED (Read Only)	NOT USED	S01	MONITOR ENABLED(Read Only)
1	BC FRAME IN PROGRESS (Read Only)	NOT USED	S00	MONITOR TRIGGERED (Read Only)
0 (LSB)	BC MESSAGE IN PROGRESS (Read Only)	RT MESSAGE IN PROGRESS (Enhanced mode only,Read Only)	RT MESSAGE IN PROGRESS (Read Only)	MONITOR ACTIVE (Read Only)

TABLE 5. CONFIGURATION REGISTER #2 (READ/WRITE 02H)	
BIT	**DESCRIPTION**
15(MSB)	ENHANCED INTERRUPTS
14	RAM PARITY ENABLE
13	BUSY LOOKUP TABLE ENABLE
12	RX SA DOUBLE BUFFER ENABLE
11	OVERWRITE INVALID DATA
10	256-WORD BOUNDARY DISABLE
9	TIME TAG RESOLUTION 2
8	TIME TAG RESOLUTION 1
7	TIME TAG RESOLUTION 0
6	CLEAR TIME TAG ON SYNCHRONIZE
5	LOAD TIME TAG ON SYNCHRONIZE
4	INTERRUPT STATUS AUTO CLEAR
3	LEVEL/PULSE* INTERRUPT REQUEST
2	CLEAR SERVICE REQUEST
1	ENHANCED RT MEMORY MANAGEMENT
0(LSB)	SEPARATE BROADCAST DATA

TABLE 6. START/RESET REGISTER (WRITE 03H)	
BIT	**DESCRIPTION**
15(MSB)	RESERVED
14	RESERVED
13	RESERVED
12	RESERVED
11	CLEAR RT HALT
10	CLEAR SELF-TEST REGISTER
9	INITIATE RAM SELF-TEST
8	RESERVED
7	INITIATE PROTOCOL SELF-TEST
6	BC/MT STOP-ON-MESSAGE
5	BC STOP-ON-FRAME
4	TIME TAG TEST CLOCK
3	TIME TAG RESET
2	INTERRUPT RESET
1	BC/MT START
0(LSB)	RESET

TABLE 7. BC/RT COMMAND STACK POINTER REG. (READ 03H)	
BIT	**DESCRIPTION**
15(MSB)	COMMAND STACK POINTER 15
•	•
•	•
•	•
0(LSB)	COMMAND STACK POINTER 0

TABLE 8. BC CONTROL WORD REGISTER (READ/WRITE 04H)	
BIT	**DESCRIPTION**
15(MSB)	RESERVED
14	MESSAGE ERROR MASK
13	SERVICE REQUEST BIT MASK
12	BUSY BIT MASK
11	SUBSYSTEM FLAG BIT MASK
10	TERMINAL FLAG BIT MASK
9	RESERVED BITS MASK
8	RETRY ENABLED
7	BUS CHANNEL A/$\overline{B}$
6	OFF-LINE SELF-TEST
5	MASK BROADCAST BIT
4	EOM INTERRUPT ENABLE
3	1553A/B SELECT
2	MODE CODE FORMAT
1	BROADCAST FORMAT
0(LSB)	RT-to-RT FORMAT

TABLE 9. RT SUBADDRESS CONTROL WORD (READ/WRITE 04H)	
BIT	**DESCRIPTION**
15(MSB)	RX: DOUBLE BUFFER ENABLE
14	TX: EOM INT
13	TX: CIRC BUF INT
12	TX: MEMORY MANAGEMENT 2 (MM2)
11	TX: MEMORY MANAGEMENT 1 (MM1)
10	TX: MEMORY MANAGEMENT 0 (MM0)
9	RX: EOM INT
8	RX: CIRC BUF INT
7	RX: MEMORY MANAGEMENT 2 (MM2)
6	RX: MEMORY MANAGEMENT 1 (MM1)
5	RX: MEMORY MANAGEMENT 0 (MM0)
4	BCST: EOM INT
3	BCST: CIRC BUF INT
2	BCST:MEMORY MANAGEMENT 2 (MM2)
1	BCST: MEMORY MANAGEMENT 1 (MM1)
0(LSB)	BCST: MEMORY MANAGEMENT 0 (MM0)

TABLE 10. TIME TAG REGISTER (READ/WRITE 05H)	
BIT	**DESCRIPTION**
15(MSB)	TIME TAG 15
•	•
•	•
•	•
0(LSB)	TIME TAG 0

TABLE 11. INTERRUPT STATUS REGISTER #1 (READ 06H)

BIT	DESCRIPTION
15(MSB)	MASTER INTERRUPT
14	RAM PARITY ERROR
13	TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	HANDSHAKE FAIL
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	BC STATUS SET / RT MODE CODE / MT PATTERN TRIGGER
0(LSB)	END OF MESSAGE

TABLE 12. CONFIGURATION REGISTER #3 (READ/WRITE 07H)

BIT	DESCRIPTION
15(MSB)	ENHANCED MODE ENABLE
14	BC/RT COMMAND STACK SIZE 1
13	BC/RT COMMAND STACK SIZE 0
12	MT COMMAND STACK SIZE 1
11	MT COMMAND STACK SIZE 0
10	MT DATA STACk SIZE 2
9	MT DATA STACk SIZE 1
8	MT DATA STACk SIZE 0
7	ILLEGALIZATION DISABLED
6	OVERRIDE MODE T/$\overline{R}$ ERROR
5	ALTERNATE STATUS WORD ENABLE
4	ILLEGAL RX TRANSFER DISABLE
3	BUSY RX TRANSFER DISABLE
2	$\overline{\text{RTFAIL}}$ / $\overline{\text{RTFLAG}}$ WRAP ENABLE
1	1553A MODE CODES ENABLE
0(LSB)	ENHANCED MODE CODE HANDLING

TABLE 13. CONFIGURATION REGISTER #4 (READ/WRITE 08H)

BIT	DESCRIPTION
15(MSB)	EXTERNAL BIT WORD ENABLE
14	INHIBIT BIT WORD IF BUSY
13	MODE COMMAND OVERRIDE BUSY
12	EXPANDED BC CONTROL WORD ENABLE
11	BROADCAST MASK ENA/$\overline{\text{XOR}}$
10	RETRY IF -A AND M.E.
9	RETRY IF STATUS SET
8	1ST RETRY ALT/$\overline{\text{SAME}}$ BUS
7	2ND RETRY ALT/$\overline{\text{SAME}}$ BUS
6	VALID M.E./NO DATA
5	VALID BUSY/NO DATA
4	MT TAG GAP OPTION
3	LATCH RT ADRRESS WITH CONFIG #5
2	TEST MODE 2
1	TEST MODE 1
0(LSB)	TEST MODE 0

TABLE 14. CONFIGURATION REGISTER #5 (READ/WRITE 09H)

BIT	DESCRIPTION
15(MSB)	12 / $\overline{16}$ MHZ CLOCK SELECT
14	SINGLE-ENDED SELECT
13	EXTERNAL TX INHIBIT A
12	EXTERNAL TX INHIBIT B
11	EXPANDED CROSSING ENABLED
10	RESPONSE TIMEOUT SELECT 1
9	RESPONSE TIMEOUT SELECT 0
8	GAP CHECK ENABLED
7	BROADCAST DISABLED
6	RT ADDRESS LATCH/$\overline{\text{TRANSPARENT}}$
5	RT ADDRESS 4
4	RT ADDRESS 3
3	RT ADDRESS 2
2	RT ADDRESS 1
1	RT ADDRESS 0
0(LSB)	RT ADDRESS PARITY

TABLE 15. RT / MONITOR DATA STACK ADDRESS REGISTER (READ/WRITE 0AH)

BIT	DESCRIPTION
15(MSB)	RT / MONITOR DATA STACK ADDRESS 15
•	•
•	•
•	•
0(LSB)	RT / MONITOR DATA STACK ADDRESS 0

TABLE 16. BC FRAME TIME REMAINING REGISTER (READ/WRITE 0BH)	
BIT	**DESCRIPTION**
15(MSB)	BC FRAME TIME REMAINING 15
•	•
•	•
•	•
0(LSB)	BC FRAME TIME REMAINING 0

Note: resolution = 100 µs per LSB

TABLE 17. BC MESSAGE TIME REMAINING REGISTER (READ/WRITE 0CH)	
BIT	**DESCRIPTION**
15(MSB)	BC MESSAGE TIME REMAINING 15
•	•
•	•
•	•
0(LSB)	BC MESSAGE TIME REMAINING 0

Note: resolution = 1 µs per LSB

TABLE 18. BC FRAME TIME / RT LAST COMMAND / MT TRIGGER REGISTER (READ/WRITE 0DH)	
BIT	**DESCRIPTION**
15(MSB)	BIT 15
•	•
•	•
•	•
0(LSB)	BIT 0

TABLE 19. RT STATUS WORD REGISTER (READ/WRITE 0EH)	
BIT	**DESCRIPTION**
15(MSB)	LOGIC “0”
14	LOGIC “0”
13	LOGIC “0”
12	LOGIC “0”
11	LOGIC “0”
10	MESSAGE ERROR
9	INSTRUMENTATION
8	SERVICE REQUEST
7	RESERVED
6	RESERVED
5	RESERVED
4	BROADCAST COMMAND RECEIVED
3	BUSY
2	SUBSYSTEM FLAG
1	DYNAMIC BUS CONTROL ACCEPT
0(LSB)	TERMINAL FLAG

TABLE 20. RT BIT WORD REGISTER (WRITE 0FH)	
BIT	**DESCRIPTION**
15(MSB)	TRANSMITTER TIMEOUT
14	LOOP TEST FAILURE B
13	LOOP TEST FAILURE A
12	HANDSHAKE FAILURE
11	TRANSMITTER SHUTDOWN B
10	TRANSMITTER SHUTDOWN A
9	TERMINAL FLAG INHIBITED
8	BIT TEST FAIL
7	HIGH WORD COUNT
6	LOW WORD COUNT
5	INCORRECT SYNC RECEIVED
4	PARITY / MANCHESTER ERROR RECEIVED
3	RT-to-RT GAP / SYNCH / ADDRESS ERROR
2	RT-to-RT NO RESPONSE ERROR
1	RT-to-RT 2ND COMMAND WORD ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

TABLE 21. CONFIGURATION REGISTER #6 (READ/WRITE 18H)	
BIT	**DESCRIPTION**
15(MSB)	ENHANCED BUS CONTROLLER
14	ENHANCED CPU ACCESS
13	COMMAND STACK POINTER INCREMENT ON EOM (RT, MT)
12	GLOBAL CIRCULAR BUFFER ENABLE
11	GLOBAL CIRCULAR BUFFER SIZE 2
10	GLOBAL CIRCULAR BUFFER SIZE 1
9	GLOBAL CIRCULAR BUFFER SIZE 0
8	DISABLE INVALID MESSAGES TO INTERRUPT STATUS QUEUE
7	DISABLE VALID MESSAGES TO INTERRUPT STATUS QUEUE
6	INTERRUPT STATUS QUEUE ENABLE
5	RT ADDRESS SOURCE
4	ENHANCED MESSAGE MONITOR
3	RESERVED
2	64-WORD REGISTER SPACE
1	CLOCK SELECT 1
0(LSB)	CLOCK SELECT 0

TABLE 22. CONFIGURATION REGISTER #7 (READ/WRITE 19H)	
BIT	**DESCRIPTION**
15(MSB)	MEMORY MANAGEMENT BASE ADDRESS 15
14	MEMORY MANAGEMENT BASE ADDRESS 14
13	MEMORY MANAGEMENT BASE ADDRESS 13
12	MEMORY MANAGEMENT BASE ADDRESS 12
11	MEMORY MANAGEMENT BASE ADDRESS 11
10	MEMORY MANAGEMENT BASE ADDRESS 10
9	RESERVED
8	RESERVED
7	RESERVED
6	RESERVED
5	RESERVED
4	RT HALT ENABLE
3	1553B RESPONSE TIME
2	ENHANCED TIMETAG SYNCHRONIZE
1	ENHANCED BC WATCHDOG TIMER ENABLED
0(LSB)	MODE CODE RESET / $\overline{\text{INCMD}}$ SELECT

TABLE 23. BC CONDITION REGISTER (READ 1BH)	
BIT	**DESCRIPTION**
15(MSB)	ALWAYS
14	RETRY 1
13	RETRY 0
12	BAD MESSAGE
11	MESSAGE STATUS SET
10	GOOD BLOCK TRANSFER
9	FORMAT ERROR
8	NO RESPONSE
7	GENERAL PURPOSE FLAG 7
6	GENERAL PURPOSE FLAG 6
5	GENERAL PURPOSE FLAG 5
4	GENERAL PURPOSE FLAG 4
3	GENERAL PURPOSE FLAG 3
2	GENERAL PURPOSE FLAG 2
1	LESS THAN FLAG / GENERAL PURPOSE FLAG 1
0(LSB)	EQUAL FLAG / GENERAL PURPOSE FLAG 1

TABLE 24. BC GENERAL PURPOSE FLAG REGISTER (WRITE 1BH)	
BIT	**DESCRIPTION**
15(MSB)	CLEAR GENERAL PURPOSE FLAG 7
14	CLEAR GENERAL PURPOSE FLAG 6
13	CLEAR GENERAL PURPOSE FLAG 5
12	CLEAR GENERAL PURPOSE FLAG 4
11	CLEAR GENERAL PURPOSE FLAG 3
10	CLEAR GENERAL PURPOSE FLAG 2
9	CLEAR GENERAL PURPOSE FLAG 1
8	CLEAR GENERAL PURPOSE FLAG 0
7	SET GENERAL PURPOSE FLAG 7
6	SET GENERAL PURPOSE FLAG 6
5	SET GENERAL PURPOSE FLAG 5
4	SET GENERAL PURPOSE FLAG 4
3	SET GENERAL PURPOSE FLAG 3
2	SET GENERAL PURPOSE FLAG 2
1	SET GENERAL PURPOSE FLAG 1
0(LSB)	SET GENERAL PURPOSE FLAG 0

TABLE 25. BIT TEST STATUS FLAG REGISTER (READ 1CH)	
BIT	**DESCRIPTION**
15(MSB)	PROTOCOL BUILT-IN TEST COMPLETE
14	PROTOCOL BUILT-IN TEST IN-PROGRESS
13	PROTOCOL BUILT-IN TEST PASSED
12	PROTOCOL BUILT-IN TEST ABORT
11	LOGIC ”1”
10	LOGIC ”0”
9	LOGIC ”0”
8	LOGIC ”0”
7	RAM BUILT-IN TEST COMPLETE
6	RAM BUILT-IN TEST IN-PROGRESS
5	RAM BUILT-IN TEST IN-PASSED
4	LOGIC ”0”
3	LOGIC ”0”
2	LOGIC ”0”
1	LOGIC ”0”
0(LSB)	LOGIC ”0”

TABLE 26. INTERRUPT MASK REGISTER #2 (READ/WRITE 1DH)	
BIT	**DESCRIPTION**
15(MSB)	NOT USED
14	BC OP CODE PARITY ERROR
13	ILLEGAL COMMAND
12	GENERAL PURPOSE QUEUE / INTERRUPT STATUS QUEUE ROLLOVER
11	CALL STACK POINTER REGISTER ERROR
10	BC TRAP OP CODE
9	RT COMMAND STACK 50% ROLLOVER
8	RT CIRCULAR BUFFER 50% ROLLOVER
7	MONITOR COMMAND STACK 50% ROLLOVER
6	MONITOR DATA STACK 50% ROLLOVER
5	ENHANCED BC IRQ3
4	ENHANCED BC IRQ2
3	ENHANCED BC IRQ1
2	ENHANCED BC IRQ0
1	BIT TEST COMPLETE
0(LSB)	NOT USED

TABLE 27. INTERRUPT STATUS REGISTER #2 (READ 1EH)	
BIT	**DESCRIPTION**
15(MSB)	MASTER INTERRUPT
14	BC OP CODE PARITY ERROR
13	ILLEGAL COMMAND
12	GENERAL PURPOSE QUEUE / INTERRUPT STATUS QUEUE ROLLOVER
11	CALL STACK POINTER REGISTER ERROR
10	BC TRAP OP CODE
9	RT COMMAND STACK 50% ROLLOVER
8	RT CIRCULAR BUFFER 50% ROLLOVER
7	MONITOR COMMAND STACK 50% ROLLOVER
6	MONITOR DATA STACK 50% ROLLOVER
5	ENHANCED BC IRQ3
4	ENHANCED BC IRQ2
3	ENHANCED BC IRQ1
2	ENHANCED BC IRQ0
1	BIT TEST COMPLETE
0(LSB)	INTERRUPT CHAIN BIT

TABLE 28. BC GENERAL PURPOSE QUEUE POINTER REGISTER RT, MT INTERRUPT STATUS QUEUE POINTER REGISTER (READ/WRITE1FH)	
BIT	**DESCRIPTION**
15(MSB)	QUEUE POINTER BASE ADDRESS 15
14	QUEUE POINTER BASE ADDRESS 14
13	QUEUE POINTER BASE ADDRESS 13
12	QUEUE POINTER BASE ADDRESS 12
11	QUEUE POINTER BASE ADDRESS 11
10	QUEUE POINTER BASE ADDRESS 10
9	QUEUE POINTER BASE ADDRESS 9
8	QUEUE POINTER BASE ADDRESS 8
7	QUEUE POINTER BASE ADDRESS 7
6	QUEUE POINTER BASE ADDRESS 6
5	QUEUE POINTER ADDRESS 5
4	QUEUE POINTER ADDRESS 4
3	QUEUE POINTER ADDRESS 3
2	QUEUE POINTER ADDRESS 2
1	QUEUE POINTER ADDRESS 1
0(LSB)	QUEUE POINTER ADDRESS 0

NOTE: TABLES 29 TO 35 ARE NOT REGISTERS, BUT THEY ARE WORDS STORED IN RAM.

TABLE 29. BC MODE BLOCK STATUS WORD	
BIT	**DESCRIPTION**
15(MSB)	EOM
14	SOM
13	CHANNEL B/$\overline{A}$
12	ERROR FLAG
11	STATUS SET
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	MASKED STATUS SET
6	RETRY COUNT 1
5	RETRY COUNT 0
4	GOOD DATA BLOCK TRANSFER
3	WRONG STATUS ADDRESS / NO GAP
2	WORD COUNT ERROR
1	INCORRECT SYNC TYPE
0(LSB)	INVALID WORD

TABLE 30. RT MODE BLOCK STATUS WORD	
BIT	**DESCRIPTION**
15(MSB)	EOM
14	SOM
13	CHANNEL B/$\overline{A}$
12	ERROR FLAG
11	RT-to-RT FORMAT
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	DATA STACK ROLLOVER
6	ILLEGAL COMMAND WORD
5	WORD COUNT ERROR
4	INCORRECT DATA SYNC
3	INVALID WORD
2	RT-to-RT GAP / SYNC / ADDRESS ERROR
1	RT-to-RT 2ND COMMAND ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

TABLE 31. 1553 COMMAND WORD	
BIT	**DESCRIPTION**
15(MSB)	REMOTE TERMINAL ADDRESS BIT 4
14	REMOTE TERMINAL ADDRESS BIT 3
13	REMOTE TERMINAL ADDRESS BIT 2
12	REMOTE TERMINAL ADDRESS BIT 1
11	REMOTE TERMINAL ADDRESS BIT 0
10	TRANSMIT / $\overline{\text{RECEIVE}}$
9	SUBADDRESS / MODE BIT 4
8	SUBADDRESS / MODE BIT 3
7	SUBADDRESS / MODE BIT 2
6	SUBADDRESS / MODE BIT 1
5	SUBADDRESS / MODE BIT 0
4	DATA WORD COUNT / MODE CODE BIT 4
3	DATA WORD COUNT / MODE CODE BIT 3
2	DATA WORD COUNT / MODE CODE BIT 2
1	DATA WORD COUNT / MODE CODE BIT 1
0(LSB)	DATA WORD COUNT / MODE CODE BIT 0

TABLE 32. WORD MONITOR IDENTIFICATION WORD	
BIT	**DESCRIPTION**
15(MSB)	GAP TIME (MSB)
•	•
•	•
•	•
8	GAP TIME (LSB)
7	WORD FLAG
6	$\overline{\text{THIS RT}}$
5	$\overline{\text{BROADCAST}}$
4	ERROR
3	COMMAND / $\overline{\text{DATA}}$
2	CHANNEL B/$\overline{A}$
1	CONTIGUOUS DATA / $\overline{\text{GAP}}$
0(LSB)	$\overline{\text{MODE\_CODE}}$

TABLE 33. MESSAGE MONITOR MODE BLOCK STATUS WORD	
BIT	**DESCRIPTION**
15(MSB)	EOM
14	SOM
13	CHANNEL B/$\overline{A}$
12	ERROR FLAG
11	RT-to-RT TRANSFER
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	GOOD DATA BLOCK TRANSFER
7	DATA STACK ROLLOVER
6	RESERVED
5	WORD COUNT ERROR
4	INCORRECT SYNC
3	INVALID WORD
2	RT-to-RT GAP / SYNC / ADDRESS ERROR
1	RT-to-RT 2ND COMMAND ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

TABLE 34. RT/MONITOR INTERRUPT STATUS WORD (FOR INTERRUPT STATUS QUEUE)		
BIT	**DEFINTION FOR MESSAGE INTERRUPT EVENT**	**DEFINITION FOR NON-MESSAGE INTERRUPT EVENT**
15	TRANSMITTER TIMEOUT	NOT USED
14	ILLEGAL COMMAND	NOT USED
13	MONITOR DATA STACK 50% ROLLOVER	NOT USED
12	MONITOR DATA STACK ROLLOVER	NOT USED
11	RT CIRCULAR BUFFER 50% ROLLOVER	NOT USED
10	RT CIRCULAR BUFFER ROLLOVER	NOT USED
9	MONITOR COMMAND (DESCRIPTOR) STACK 50% ROLLOVER	NOT USED
8	MONITOR COMMAND (DESCRIPTOR) STACK ROLLOVER	NOT USED
7	RT COMMAND (DESCRIPTOR) STACK 50% ROLLOVER	NOT USED
6	RT COMMAND (DESCRIPTOR) STACK ROLLOVER	NOT USED
5	HANDSHAKE FAIL	NOT USED
4	FORMAT ERROR	TIME TAG ROLLOVER
3	MODE CODE INTERRUPT	RT ADDRESS PARITY ERROR
2	SUBADDRESS CONTROL WORD EOM	PROTOCOL SELF-TEST COMPLETE
1	END-OF-MESSAGE (EOM)	RAM PARITY ERROR
0	“1” FOR MESSAGE INTERRUPT EVENT ”0” FOR NON-MESSAGE INTERRUPT EVENT	

TABLE 35. 1553B STATUS WORD	
BIT	**DESCRIPTION**
15(MSB)	REMOTE TERMINAL ADDRESS BIT 4
14	REMOTE TERMINAL ADDRESS BIT 3
13	REMOTE TERMINAL ADDRESS BIT 2
12	REMOTE TERMINAL ADDRESS BIT 1
11	REMOTE TERMINAL ADDRESS BIT 0
10	MESSAGE ERROR
9	INSTRUMENTATION
8	SERVICE REQUEST
7	RESERVED
6	RESERVED
5	RESERVED
4	BROADCAST COMMAND RECEIVED
3	BUSY
2	SUBSYSTEM FLAG
1	DYNAMIC BUS CONTROL ACCEPTANCE
0(LSB)	TERMINAL FLAG

NON-TEST REGISTER FUNCTION SUMMARY

A summary of the Enhanced Mini-ACE's 24 non-test registers follows.

Interrupt Mask Registers #1 and #2 are used to enable and disable interrupt requests for various events and conditions.

Configuration Registers #1 and #2 are used to select the Enhanced Mini-ACE's mode of operation, and for software control of RT Status Word bits, Active Memory Area, BC Stop-On-Error, RT Memory Management mode selection, and control of the Time Tag operation.

Start/Reset Register is used for "command" type functions such as software reset, BC/MT Start, Interrupt reset, Time Tag Reset, Time Tag Register Test, Initiate protocol self-test, Initiate RAM self-test, Clear self-test register, and Clear RT Halt. The Start/Reset Register also includes provisions for stopping the BC in its auto-repeat mode, either at the end of the current message or at the end of the current BC frame.

BC/RT Command Stack Register allows the host CPU to determine the pointer location for the current or most recent message.

BC Instruction List Pointer Register may be read to determine the current location of the Instruction List Pointer for the Enhanced BC mode.

BC Control Word/RT Subaddress Control Word Register: In BC mode, allows host access to the current word or most recent BC Control Word. The BC Control Word contains bits that select

the active bus and message format, enable off-line self-test, masking of Status Word bits, enable retires and interrupts, and specify MIL-STD-1553A or -1553B error handling. In RT mode, this register allows host access to the current or most recent Subaddress Control Word. The Subaddress Control Word is used to select the memory management scheme and enable interrupts for the current message.

Time Tag Register maintains the value of a real-time clock. The resolution of this register is programmable from among 2, 4, 8, 16, 32, and 64 µs/LSB. The Start-of-Message (SOM) and End-of-Message (EOM) sequences in BC, RT, and Message Monitor modes cause a write of the current value of the Time Tag Register to the stack area of the RAM.

Interrupt Status Register #1 and #2 allow the host processor to determine the cause of an interrupt request by means of one or two read accesses. The interrupt events of the two Interrupt Status Registers are mapped to correspond to the respective bit positions in the two Interrupt Mask Registers. Interrupt Status Register #2 contains an INTERRUPT CHAIN bit, used to indicate an interrupt event from Interrupt Status Register #1.

Configuration Registers #3, #4, and #5 are used to enable many of the Enhanced Mini-ACE's advanced features that were implemented by the prior generation products, the ACE and Mini-ACE (Plus). For BC, RT, and MT modes, use of the ENHANCED MODE enables the various read-only bits in Configuration Register #1. For BC mode, ENHANCED mode features include the expanded BC Control Word and BC Block Status Word, additional Stop-On-Error and Stop-On-Status Set functions, frame auto-repeat, programmable intermessage gap times, automatic retires, expanded Status Word Masking, and the capability to generate interrupts following the completion of any selected message. For RT mode, the enhanced mode features include the expanded RT Block Status Word, combined RT/Selective Message Monitor mode, automatic setting of the TERMINAL FLAG Status Word bit following a loop test failure; the double buffering scheme for individual receive (broadcast) subaddresses, and the alternate (fully software programmable) RT Status Word. For MT mode, use of the enhanced mode enables the Selective Message Monitor, the combined RT/Selective Monitor modes, and the monitor triggering capability.

RT/Monitor Data Stack Address Register provides a read/writable indication of the last data word stored for RT or Monitor modes.

BC Frame Time Remaining Register provides a read-only indication of the time remaining in the current BC frame. In the enhanced BC mode, this timer may be used for minor or major frame control, or as a watchdog timer for the BC message sequence control processor. The resolution of this register is 100 µs/LSB.

BC Time Remaining to Next Message Register provides a read-only indication of the time remaining before the start of the next message in a BC frame. In the enhanced BC mode, this timer may be also be used for the BC message sequence control processor's Delay (DLY) instruction, or for minor or major frame control. The resolution of this register is 1 µs/LSB.

BC Frame Time/ RT Last Command /MT Trigger Word Register. In BC mode, this register is used to program the BC frame time, for use in the frame auto-repeat mode. The resolution of this register is 100 µs/LS, with a range up to 6.55 seconds. In RT mode, this register stores the current (or most previous) 1553 Command Word processed by the Enhanced Mini-ACE RT. In the Word Monitor mode, this register is used to specify a 16-bit Trigger (Command) Word. The Trigger Word may be used to start or stop the monitor, or to generate interrupts.

BC Initial Instruction List Pointer Register enables the host to assign the starting address for the enhanced BC Instruction List.

RT Status Word Register and BIT Word Registers provide read-only indications of the RT Status and BIT Words.

Test Mode Registers 0-7. These registers are included for factory test. In normal operation, these registers do not need to be accessed by the host processor.

Configuration Registers #6 and #7 are used to enable the Enhanced Mini-ACE features that extend beyond the architecture of the ACE/Mini-ACE (Plus). These include the Enhanced BC mode; RT Global Circular Buffer (including buffer size); the RT/MT Interrupt Status Queue, including valid/invalid message filtering; enabling a software-assigned RT address; clock frequency selection; a base address for the "non-data" portion of Enhanced Mini-ACE memory; LSB filtering for the Synchronize (with data) time tag operations; and enabling a watchdog timer for the Enhanced BC message sequence control engine.

BC Condition Code Register is used to enable the host processor to read the current value of the Enhanced BC Message Sequence Control Engine's condition flags.

BC General Purpose Flag Register allows the host processor to be able to set, clear, or toggle any of the Enhanced BC Message Sequence Control Engine's General Purpose condition flags.

BIT Test Status Register is used to provide read-only access to the status of the protocol and RAM built-in self-tests (BIT).

BC General Purpose Queue Pointer provides a means for initializing the pointer for the General Purpose Queue, for the Enhanced BC mode. In addition, this register enables the host to determine the current location of the General Purpose Queue pointer, which is incremented internally by the Enhanced BC message sequence control engine.

RT/MT Interrupt Status Queue Pointer Register provides a means for initializing the pointer for the Interrupt Status Queue, for RT, MT, and RT/MT modes. In addition, this register enables the host to determine the current location of the Interrupt Status Queue pointer, which is incremented by the RT/MT message

BUS CONTROLLER (BC) ARCHITECTURE

The BC functionality for the Enhanced Mini-ACE includes two separate architectures: (1) the older, non-Enhanced mode, which provides complete compatibility with the previous ACE and Mini-ACE (Plus) generation products; and (2) the newer, Enhanced BC mode. The Enhanced BC mode offers several new powerful architectural features. These includes the incorporation of a highly autonomous BC message sequence control engine, which greatly serves to offload the operation of the host CPU.

The Enhanced BC's message sequence control engine provides a high degree of flexibility for implementing major and minor frame scheduling; capabilities for inserting asynchronous messages in the middle of a frame; to separate 1553 message data from control/status data for the purpose of implementing double buffering and performing bulk data transfers; for implementing message retry schemes, including the capability for automatic bus channel switchover for failed messages; and for reporting various conditions to the host processor by means of 4 user-defined interrupts and a general purpose queue.

In both the non-Enhanced and Enhanced BC modes, the Enhanced Mini-ACE BC implements all MIL-STD-1553B message formats. Message format is programmable on a message-by-message basis by means the BC Control Word and the $\overline{T/R}$ bit of the Command Word for the respective message. The BC Control Word allows 1553 message format, 1553A/B type RT, bus channel, self-test, and Status Word masking to be specified on an individual message basis. In addition, automatic retries and/or interrupt requests may be enabled or disabled for individual messages. The BC performs all error checking required by MIL-STD-1553B. This includes validation of response time, sync type and sync encoding, Manchester II encoding, parity, bit count, word count, Status Word RT Address field, and various RT-to-RT transfer errors. The Enhanced Mini-ACE BC response timeout value is programmable with choices of 18, 22, 50, and 130 µs. The longer response timeout values allow for operation over long buses and/or the use of repeaters.

In its non-Enhanced mode, the Enhanced Mini-ACE may be programmed to process BC frames of up to 512 messages with no processor intervention. In the Enhanced BC mode, there is no explicit limit to the number of messages that may be processed in a frame. In both modes, it is possible to program for either single frame or frame auto-repeat operation. In the auto-repeat mode, the frame repetition rate may be controlled either internally, using a programmable BC frame timer, or from an external trigger input.

ENHANCED BC MODE: MESSAGE SEQUENCE CONTROL

One of the major new architectural features of the Enhanced Mini-ACE series is its advanced capability for BC message sequence control. The Enhanced Mini-ACE supports highly autonomous BC operation, which greatly offloads the operation of the host processor.

The operation of the Enhanced Mini-ACE's message sequence control engine is illustrated in FIGURE 2. The BC message sequence control involves an instruction list pointer register; an instruction list which contains multiple 2-word entries; a message control/status stack, which contains multiple 8-word or 10-word descriptors; and data blocks for individual messages.

The initial value of the instruction list pointer register is initialized by the host processor (via Register 0D), and is incremented by the BC message sequence processor (host readable via Register 03). During operation, the message sequence control processor fetches the operation referenced by the instruction list pointer register from the instruction list.

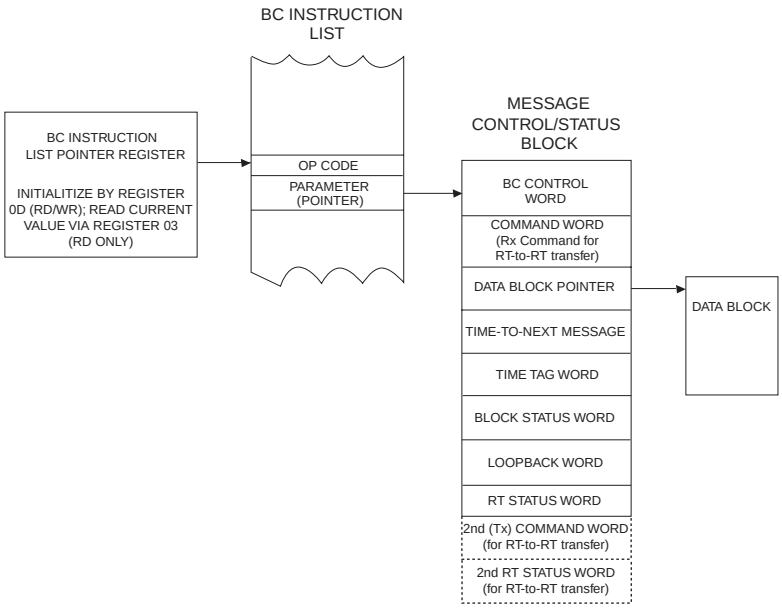


FIGURE 2. BC MESSAGE SEQUENCE CONTROL

Note that the pointer parameter referencing the first word of a message's control/status block (the BC Control Word) must contain an address value that is **modulo 8**. Also, note that if the message is an RT-to-RT transfer, the pointer parameter must contain an address value that is **modulo 16**.

OP CODES

The instruction list pointer register references a pair of words in the BC instruction list: an op code word, followed by a parameter word. The format of the op code word, which is illustrated in FIGURE 3, includes a 5-bit op code field and a 5-bit condition code field. The op code identifies the instruction to be executed by the BC message sequence controller.

Most of the operations are conditional, with execution dependent on the contents of the condition code field. Bits 3-0 of the condition code field identifies a particular condition. Bit 4 of the condition code field identifies the logic sense ("1" or "0") of the selected condition code on which the conditional execution is dependent. TABLE 36 lists all the op codes, along with their respective mnemonic, code value, parameter, and description. TABLE 37 defines all the condition codes.

Eight of the condition codes (8 through F) are set or cleared as the result of the most recent message. The other eight are defined as "General Purpose" condition codes GP0 through GP7. There are three mechanisms for programming the values of the General Purpose Condition Code bits: (1) They may be set, cleared, or toggled by the host processor, by means of the BC GENERAL PURPOSE FLAG REGISTER; (2) they may be set, cleared, or toggled by the BC message sequence control processor, by means of the GP Flag Bits (FLG) instruction; and (3) GP0 and GP1 only (but none of the others) may be set or cleared by means of the BC message sequence control processor's Compare Frame Timer (CFT) or Compare Message Timer (CMT) instructions.

The host processor also has read-only access to the BC condition codes by means of the BC CONDITION CODE REGISTER.

Note that four (4) instructions are **unconditional**. These are Compare to Frame Timer (CFT), Compare to Message Timer (CMT), GP Flag Bits (FLG), and Execute and Flip (XQF). For these instructions, the Condition Code Field is "don't care". That is, these instructions are **always** executed, regardless of the result of the condition code test.

All of the other instructions are conditional. That is, they will only be executed if the condition code specified by the condition code field in the op code word tests true. If the condition code field tests false, the instruction list pointer will skip down to the next instruction.

As shown in TABLE 36, many of the operations include a single-word parameter. For an XEQ (execute message) operation, the parameter is a pointer to the start of the message's Control / Status block. For other operations, the parameter may be an address, a time value, an interrupt pattern, a mechanism to set or clear general purpose flag bits, or an immediate value. For several op codes, the parameter is "don't care" (not used).

As described above, some of the op codes will cause the message sequence control processor to execute messages. In this case, the parameter references the first word of a message Control/Status block. With the exception of RT-to-RT transfer messages, all message status/control blocks are eight words long: a block control word, time-to-next-message parameter, data block pointer, command word, status word, loopback word, block status word, and time tag word.

In the case of an RT-to-RT transfer message, the size of the message control/status block increases to 16 words. However, in this case, the last six words are not used; the ninth and tenth words are for the second command word and second status word.

The third word in the message control/status block is a pointer that references the first word of the message's data word block. Note that the data word block stores only data words, which are to be either transmitted or received by the BC. By segregating data words from command words, status words, and other control and "housekeeping" functions, this architecture enables the use of convenient, usable data structures, such as circular buffers and double buffers.

Other operations support program flow control; i.e., jump and call capability. The call capability includes maintenance of a call stack which supports a maximum of four (4) entries; there is also a return instruction. In the case of a call stack overrun or underrun, the BC will issue a CALL STACK POINTER REGISTER ERROR interrupt, if enabled.

Other op codes may be used to delay for a specified time; start a new BC frame; wait for an external trigger to start a new frame; do comparisons based on frame time and time-to-next message; load the time tag or frame time registers; halt; and issue host interrupts. In the case of host interrupts, the message control processor passes a 4-bit user-defined interrupt vector to the host, by means of the Enhanced Mini-ACE's Interrupt Status Register.

The purpose of the FLG instruction is to enable the message sequence controller to set, clear, or toggle the value(s) of any or all of the eight general purpose condition flags.

The op code parity bit encompasses all sixteen bits of the op code word. This bit must be programmed for odd parity. If the message sequence control processor fetches an undefined op

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	OpCode Field					0	1	0	1	0	Condition Code Field				

code word, an op code word with even parity, or bits 9-5 of an op code word do not have a binary pattern of 01010, the message sequence control processor will immediately halt the BC's operation. In addition, if enabled, a BC TRAP OP CODE interrupt will be issued. Also, if enabled, a parity error will result in an OP CODE PARITY ERROR interrupt.

TABLE 37 describes the Condition Codes.

TABLE 36. BC OPERATIONS FOR MESSAGE SEQUENCE CONTROL

INSTRUCTION	MNEMONIC	OP CODE (HEX)	PARAMETER	CONDITIONAL OR UNCONDITIONAL	DESCRIPTION
Execute Message	XEQ	0001	Message Control / Status Block Address	Conditional	Executes the message at the specified Message Control/Status Block Address if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Jump	JMP	0002	Instruction List Addrss	Conditional	Jump to the OpCode specified in the Instruction List if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Subroutine Call	CAL	0003	Instruction List Addrss	Conditional	Jump to the OpCode specified by the Instruction List Address and push the Address of the Next OpCode on the Call Stack if the condition flag test TRUE, otherwise continue execution at the next OpCode in the instruction list. Note that the maximum depth of the subroutine call stack is **four**.
Subroutine Retrn	RTN	0004	Not Used (Don't Care)	Conditional	Return to the OpCode popped off the Call Stack if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Interrupt Request	IRQ	0006	Interrupt Bit Pattern in 4 LS bits	Conditional	Generate an interrupt if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. The passed parameter (Interrupt Bit Pattern) specifies which of the ENHANCED BC IRQ bit(s) (bits 5-2) will be set in Interrupt Status Register #2. Only the four LSBs of the passed parameter are used. A parameter where the four LSBs are logic "0" will **not** generate an interrupt.
Halt	HLT	0007	Not Used (Don't Care)	Conditional	Stop execution of the Message Sequence Control Program until a new BC Start is issued by the host if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Delay	DLY	0008	Delay Time Value (Resolution = 1µS)	Conditional	Delay the time specified by the Time parameter before executing the next OpCode if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay. The delay generated will use the Time to Next Message Timer.
Wait Until Frame Timer = 0	WFT	0009	Not Used (Don't Care)	Conditional	Wait until Frame Time counter is equal to Zero before continuing execution of the Message Sequence Control Program if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay.
Compare to Frame Timer	CFT	000A	Delay Time Value (Resolution = 100µS / LSB)	Unconditional	Compare Time Value to Frame Time Counter and set or clear the LT and EQ flag based on the results of the compare.
Compare to Message Timer	CMT	000B	Delay Time Value (Resolution = 1µS / LSB)	Unconditional	Compare Time Value to Message Time Counter and set or clear the LT and EQ flag based on the results of the compare.
GP Flag Bits	FLG	000C	Used to set, clear, or toggle GP (General Purpose) Flag bits (See description)	Unconditional	Used to set, toggle, or clear any or all of the eight general purpose flags. The table below illustrates the use of the GP Flag Bits instruction for the case of GP0 (General Purpose Flag 0). Bits 1 and 9 of the parameter byte affect flag GP1, bits 2 and 10 effect GP2, etc., according to the following rules:

Bit 8	Bit 0	Effect on GP0
0	0	No Change
0	1	Set Flag
1	0	Clear Flag
1	1	Toggle Flag

TABLE 36. BC OPERATIONS FOR MESSAGE SEQUENCE CONTROL (Cont'd)					
INSTRUCTION	**MNEMONIC**	**OP CODE (HEX)**	**PARAMETER**	**CONDITIONAL OR UNCONDITIONAL**	**DESCRIPTION**
Load Time Tag Counter	LTT	000D	Time Value. Resolution (µs/LSB) is defined by bits 9, 8, and 7 of Configuration Register #2.	Conditional	Load Time Tag Counter with Time Value if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Load Frame TimerLoad Frame	LFT	000E	Time Value (resolution = 100 µs/LSB)	Conditional	Load Frame Timer Register with the Time Value parameter if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Start Frame Timer	SFT	000F	Not Used (Don't Care)	Conditional	Start Frame Time Counter with Time Value in Time Frame register if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Time Tag Register	PPT	0010	Not Used (Don't Care)	Conditional	Push the value of the Time Tag Register on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Block Status Word	PBS	0011	Not Used (Don't Care)	Conditional	Push the Block Status Word for the most recent message on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Immediate Value	PSI	0012	Immediate Value	Conditional	Push Immediate data on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Indirect	PSM	0013	Memory Address	Conditional	Push the data stored at the specified memory location on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Wait for External Trigger	WTG	0014	Not Used (Don't Care)	Conditional	Wait for a logic "0"-to-logic "1" transition on the EXT_TRIG input signal before proceeding to the next OpCode in the instruction list if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay .
Execute and Flip	XQF	0015	Message Control / Status Block Address	Unconditional	Execute (unconditionally) the message referenced by the Message Control/Status Block Address. Following the processing of this message, if the condition flag tests TRUE, the BC will toggle bit 4 in the Message Control/Status Block Address, and store the new Message Block Address as the updated value of the parameter following the XQF instruction code. As a result, the **next** time that this line in the instruction list is executed, the Message Control/Status Block at the **updated** address (**old address XOR 0010h**), rather than the old address, will be processed. If the condition flag tests FALSE, the value of the Message Control/Status Block Address parameter will not change.

TABLE 37. CONDITION CODES

BIT CODE	NAME (BIT 4 = 0)	INVERSE (BIT 4 = 1)	FUNCTIONAL DESCRIPTION
0	LT/GP0	GT/$\overline{GP0}$	Less Than Flag set or cleared after CFT or CMT operation. Also, General Purpose Flag 0 may be set or cleared by a FLG operation.
1	EQ/GP1	NE/$\overline{GP1}$	Equal Flag set or cleared after CFT or CMT operation. Also, General Purpose Flag 1 may also be set or cleared by a FLG operation.
2 3 4 5 6 7	GP2 GP3 GP4 GP5 GP6 GP7	$\overline{GP2}$ $\overline{GP3}$ $\overline{GP4}$ $\overline{GP5}$ $\overline{GP6}$ $\overline{GP7}$	General Purpose Flags may be set, cleared, or toggled by a FLG operation. The host processor can set, clear, or toggle these flags in the same way as the FLG instruction by means of the BC GENERAL PURPOSE FLAG REGISTER.
8	NORESP	$\overline{RESP}$	NORESP indicates that an RT has either not responded or has responded later than the BC No Response Timeout time. The Enhanced Mini-ACE's No Response Timeout Time is defined per MIL-STD-1553B as the time from the mid-bit crossing of the parity bit of the last word transmitted by the BC to the mid-sync crossing of the RT Status Word. The value of the No Response Timeout value is programmable from among the nominal values 18.5, 22.5, 50.5, and 130 µs (±1 µs) by means of bits 10 and 9 of Configuration Register #5.
9	FMT ERR	$\overline{FMT\ ERR}$	FMT ERR indicates that the received portion of the most recent message contained one or more violations of the 1553 message validation criteria (sync, encoding, parity, bit count, word count, etc.), or the RT's status word received from a responding RT contained an incorrect RT address field.
A	GD BLK XFER	$\overline{GD\ BLK\ XFER}$	For the most recent message, GD BLK XFER will be set to logic "1" following completion of a valid (error-free) RT-to-BC transfer, RT-to-RT transfer, or transmit mode code with data message. This bit is set to logic "0" following an invalid message. GOOD DATA BLOCK TRANSFER is **always** logic "0" following a BC-to-RT transfer, a mode code with data, or a mode code without data. The Loop Test has **no effect** on GOOD DATA BLOCK TRANSFER. GOOD DATA BLOCK TRANSFER may be used to determine if the transmitting portion of an RT-to-RT transfer was error free.
B	MASKED STATUS BIT	$\overline{MASKED\ STATUS\ BIT}$	Indicates that one or both of the following conditions have occurred for the most recent message: (1) If one (or more) of the Status Mask bits (14 through 9) in the BC Control Word is logic "0" **and** the corresponding bit(s) is (are) set (logic "1") in the received RT Status Word. In the case of the RESERVED BITS MASK (bit 9) set to logic "0," any or all of the 3 Reserved Status Word bits being set will result in a MASKED STATUS SET condition; and/or (2) If BROADCAST MASK ENABLED/$\overline{XOR}$ (bit 11 of Configuration Register #4) is logic "1" **and** the MASK BROADCAST bit of the message's BC Control Word is logic "0" and the BROADCAST COMMAND RECEIVED bit in the received RT Status Word is logic "1.".
C	BAD MESSAGE	GOOD MESSAGE	BAD MESSAGE indicates either a format error, loop test fail, or no response error for the most recent message. Note that a "Status Set" condition has **no effect** on the "BAD MESSAGE/GOOD MESSAGE" condition code.
D E	RETRY0 RETRY1	$\overline{RETRY0}$ $\overline{RETRY01}$	These two bits reflect the retry status of the most recent message. The number of times that the message was retried is delineated by these two bits as shown below: RETRY COUNT 1 (bit 14) / RETRY COUNT 0 (bit 13) / Number of Message Retries 0 / 0 / 0 0 / 1 / 1 1 / 0 / N/A 1 / 1 / 2
F	ALWAYS	$\overline{NEVER}$	The ALWAYS bit should be set to designate an instruction as unconditional. The inverse (NEVER) bit can be used to implement a NOP instruction.

BC MESSAGE SEQUENCE CONTROL

The BC Enhanced Mini-ACE BC message sequence control capability enables a high degree of offloading of the host processor. This includes using the various timing functions to enable autonomous structuring of major and minor frames. In addition, by implementing conditional jumps and subroutine calls, the message sequence control processor greatly simplifies the insertion of asynchronous, or "out-of-band" messages.

Execute and Flip Operation. The Enhanced Mini-ACE BC's XQF, or "Execute and Flip" operation, provides some unique capabilities. Following execution of this unconditional instruction, if the condition code tests TRUE, the BC will modify the value of the current XQF instruction's pointer parameter by toggling bit 4 of the pointer. That is, if the selected condition flag tests true, the value of the parameter will be **updated** to the value = **old address XOR 0010h**. As a result, the next time that this line in the instruction list is executed, the Message Control/Status Block at the updated address (old address XOR 0010h) will be processed, rather than the one at the old address. The operation of the XQF instruction is illustrated in FIGURE 4.

There are multiple ways of utilizing the "execute and flip" instruction. One is to facilitate the implementation of a double buffering data scheme for individual messages. This allows the message sequence control processor to "ping-pong" between a pair of data buffers for a particular message. By so doing, the host processor can access one of the two Data Word blocks, while the BC reads or writes the alternate Data Word block.

A second application of the "execute and flip" capability is in conjunction with message retries. This allows the BC to not only switch buses when retrying a failed message, but to automatically switch buses **permanently** for all future times that the same message is to be processed. This not only provides a high degree of autonomy from the host CPU, but saves BC bandwidth, by eliminating the need for future attempts to process messages on an RT's failed channel.

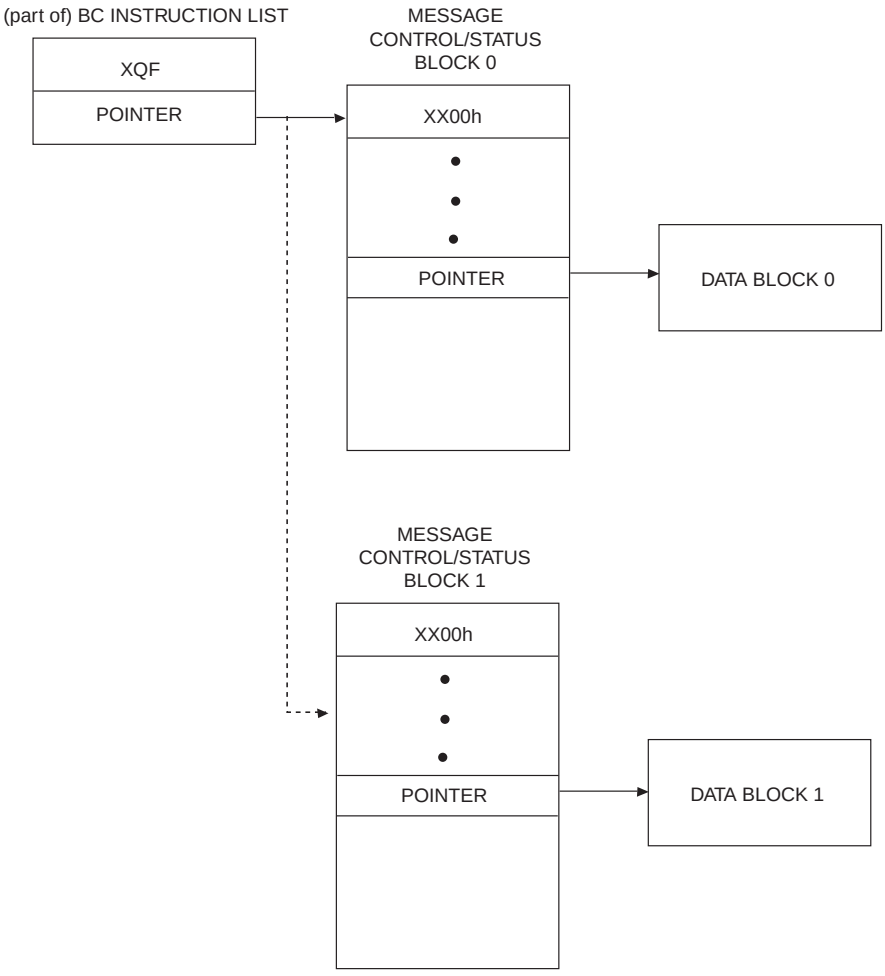


FIGURE 4. EXECUTE and FLIP (XQF) OPERATION

GENERAL PURPOSE QUEUE

General Purpose Queue. The Enhanced Mini-ACE BC allows for the creation of a general purpose queue. This data structure provides a means for the message sequence processor to convey information to the BC host. The BC op code repertoire provides mechanisms to push various items on this queue. These include the contents of the Time Tag Register, the Block Status Word for the most recent message, an immediate data value, or the contents of a specified memory address.

FIGURE 5 illustrates the operation of the BC General Purpose Queue. Note that the BC General Purpose Queue Pointer Register will always point to the **next** address location (modulo 64); that is, the location **following** the last location written by the BC message sequence control engine.

If enabled, a BC GENERAL PURPOSE QUEUE ROLLOVER interrupt will be issued when the value of the queue pointer address rolls over at a 64-word boundary. The rollover will always occur at a modulo 64 address.

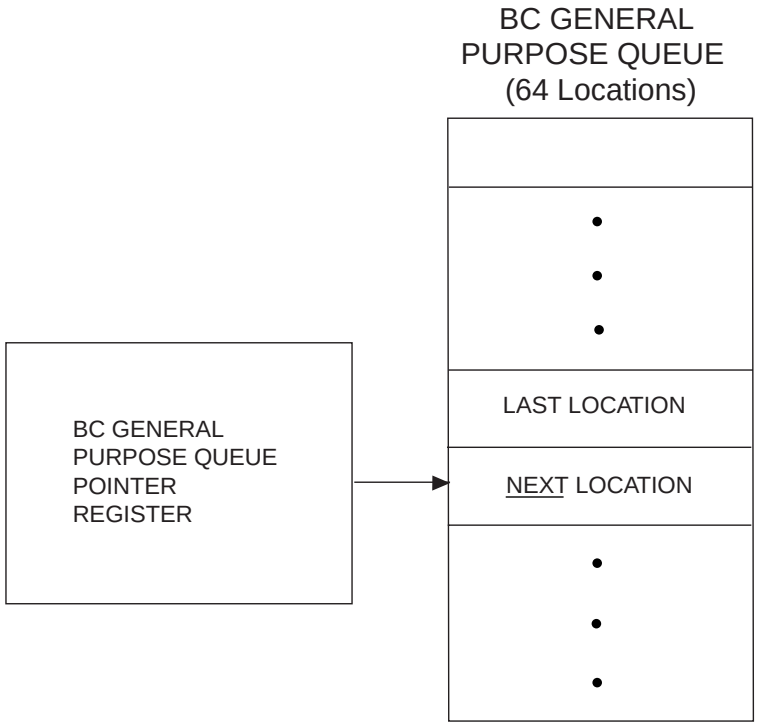


FIGURE 5. BC GENERAL PURPOSE QUEUE

REMOTE TERMINAL (RT) ARCHITECTURE

The Enhanced Mini-ACE's RT architecture builds upon that of the ACE and Mini-ACE. The Enhanced Mini-ACE provides multiprotocol support, with full compliance to all of the commonly used data bus standards, including MIL-STD-1553A, MIL-STD-1553B Notice 2, STANAG 3838, General Dynamics 16PP303, and McAirA3818, A5232, and A5690. For the Enhanced Mini-ACE RT mode, there is programmable flexibility enabling the RT to be configured to fulfill any set of system requirements. This includes the capability to meet the MIL-STD-1553A response time requirement of 2 to 5 µs, and multiple options for mode code subaddresses, mode codes, RT status word, and RT BIT word.

The Enhanced Mini-ACE RT protocol design implements all of the MIL-STD-1553B message formats and dual redundant mode codes. The design has passed validation testing for MIL-STD-1553B compliance. The Enhanced Mini-ACE RT performs comprehensive error checking including word and format validation, and checks for various RT-to-RT transfer errors. One of the main features of the Enhanced Mini-ACE RT is its choice of memory management options. These include single buffering by subaddress, double buffering for individual receive subaddresses, circular buffering by individual subaddresses, and global circular buffering for multiple (or all) subaddresses.

Other features of the Enhanced Mini-ACE RT include a set of interrupt conditions, an flexible status queue with filtering based on valid and/or invalid messages, flexible command illegalization, programmable busy by subaddress, multiple options on time tagging, and an "auto-boot" feature which allows the RT to initialize as an online RT with the busy bit set following power turn-on.

RT MEMORY ORGANIZATION

TABLE 38 illustrates a typical memory map for an Enhanced Mini-ACE RT with 4K RAM. The two Stack Pointers reside in fixed locations in the shared RAM address space: address 0100 (hex) for the Area A Stack Pointer and address 0104 for the Area B Stack Pointer. In addition to the Stack Pointer, there are several other areas of the shared RAM address space that are designated as fixed locations (all shown in **bold**). These are for the Area A and Area B lookup tables, the illegalization lookup table, the busy lookup table, and the mode code data tables.

The RT lookup tables (reference TABLE 39) provide a mechanism for allocating data blocks for individual transmit, receive, or broadcast subaddresses. The RT lookup tables include subaddress control words as well as the individual data block pointers. If command illegalization is used, address range 0300-03FF is used for command illegalizing. The descriptor stack RAM area, as well as the individual data blocks, may be located in any of the non-fixed areas in the shared RAM address space.

Note that in TABLE 38, there is no area allocated for "Stack B". This is shown for purpose of simplicity of illustration. Also, note that in TABLE 38, the allocated area for the RT command stack is 256 words. However, larger stack sizes are possible. That is, the RT command stack size may be programmed for 256 words (64 messages), 512, 1024, or 2048 words (512 messages) by means of bits 14 and 13 of Configuration Register 3.

TABLE 38. TYPICAL RT MEMORY MAP (SHOWN FOR 4K RAM)

ADDRESS (HEX)	DESCRIPTION
0000-00FF	Stack A
0100	**Stack Pointer A**
0101	**Global Circular Buffer A Pointer**
0102-0103	RESERVED
0104	**Stack Pointer B**
0105	**Global Circular Buffer B Pointer**
0106-0107	RESERVED
0108-010F	**Mode Code Selective Interrupt Table**
0110-013F	**Mode Code Data**
0140-01BF	**Lookup Table A**
01C0-023F	**Lookup Table B**
0240-0247	**Busy Bit Lookup Table**
0248-025F	(not used)
0260-027F	Data Block 0
0280-02FF	Data Block 1-4
0300-03FF	**Command Illegalizing Table**
0400-041F	Data Block 5
0420-043F	Data Block 6
•	•
•	•
•	•
0FE0-0FFF	Data Block 100

TABLE 39. RT LOOK-UP TABLES

AREA A	AREA B	DESCRIPTION	COMMENT
0140 . . . 015F	01C0 . . . 01DF	Rx(/Bcst) SA0 . . . Rx(/Bcst) SA31	Receive (/Broadcast) Lookup Pointer Table
0160 . . . 017F	01E0 . . . 01FF	Tx SA0 . . . Tx SA31	Transmit Lookup Pointer Table
0180 . . . 019F	0200 . . . 021F	Bcst SA0 . . . Bcst SA31	Broadcast Lookup Pointer Table (Optional)
01A0 . . . 01BF	0220 . . . 023F	SACW SA0 . . . SACW SA31	Subaddress Control Word Lookup Pointer Table (Optional)

RT MEMORY MANAGEMENT

The Enhanced Mini-ACE provides a variety of RT memory management capabilities. As with the ACE and Mini-ACE, the choice of memory management scheme is fully programmable on a transmit/receive/broadcast subaddress basis.

In compliance with MIL-STD-1553B Notice 2, received data from broadcast messages may be optionally separated from non-broadcast received data. For each transmit, receive or broadcast subaddress, either a single-message data block, a double buffered configuration (two alternating Data Word blocks), or a variable-sized (128 to 8192 words) subaddress circular buffer may be allocated for data storage. The memory management scheme for individual subaddresses is designated by means of the subaddress control word (reference TABLE 40).

For received data, there is also a global circular buffer mode. In this configuration, the data words received from multiple (or all) subaddresses are stored in a common circular buffer structure. Like the subaddress circular buffer, the size of the global circular buffer is programmable, with a range of 128 to 8192 data words.

The double buffering feature provides a means for the host processor to easily access the most recent, complete received block of valid Data Words for any given subaddress. In addition to helping ensure data sample consistency, the circular buffer options provide a means for greatly reducing host processor overhead for multi-message bulk data transfer applications.

End-of-message interrupts may be enabled either globally (following all messages), following error messages, on a transmit/receive/broadcast subaddress or mode code basis, or when a circular buffer reaches its midpoint (50% boundary) or lower (100%) boundary. A pair of interrupt status registers allow the host processor to determine the cause of all interrupts by means of a single read operation.

TABLE 40. RT SUBADDRESS CONTROL WORD - MEMORY MANAGEMENT OPTIONS

DOUBLE-BUFFERED OR GLOBAL CIRCULAR BUFFER (bit 15)	SUBADDRESS CONTROL WORD BITS			MEMORY MANAGEMENT SUBADDRESS BUFFER SCHEME DESCRIPTION	
	MM2	MM1	MM0		
0	0	0	0	Single Message	
1	0	0	0	For Receive or Broadcast: Double Buffered For Transmit: Single Message	
0	0	0	1	128-Word	Subaddress - specific circular buffer of specified size.
0	0	1	0	256-Word	
0	0	1	1	512-Word	
0	1	0	0	1024-Word	
0	1	0	1	2048-Word	
0	1	1	0	4096-Word	
0	1	1	1	8192-Word	
1	1	1	1	(for receive and / or broadcast subaddresses only) Global Circular Buffer: The buffer size is specified by Configuration Register #6, bits 11-9. The pointer to the global circular buffer is stored at address 0101 (for Area A) or address 0105 (for Area B)	

SINGLE BUFFERED MODE

The operation of the single buffered RT mode is illustrated in FIGURE 6. In the single buffered mode, the respective lookup table entry must be written by the host processor. Received data words are written to, or transmitted data words are read from the data word block with starting address referenced by the lookup table pointer. In the single buffered mode, the current lookup table pointer is not updated by the Enhanced Mini-ACE memory management logic. Therefore, if a subsequent message is received for the same subaddress, the **same** Data Word block will be overwritten or overread.

SUBADDRESS DOUBLE BUFFERING MODE

The Enhanced Mini-ACE provides a double buffering mechanism for received data, that may be selected on an individual subaddress basis for any or all receive (and/or broadcast) subaddresses. This is illustrated in FIGURE 7. It should be noted that the Subaddress Double Buffering mode is applicable for receive data only, **not for transmit data.** Double buffering of transmit messages may be easily implemented by software techniques.

The purpose of the subaddress double buffering mode is to provide data sample consistency to the host processor. This is accomplished by allocating **two** 32-word data word blocks for each individual receive (and/or broadcast receive) subaddress. At any given time, one of the blocks will be designated as the "active "1553 block while the other will be considered as "inactive". The data words for the next receive command to that subaddress will be stored in the active block. Following receipt of a valid message, the Enhanced Mini-ACE will automatically switch the active and inactive blocks for that subaddress. As a result, the latest, valid, complete data block is always accessible to the host processor.

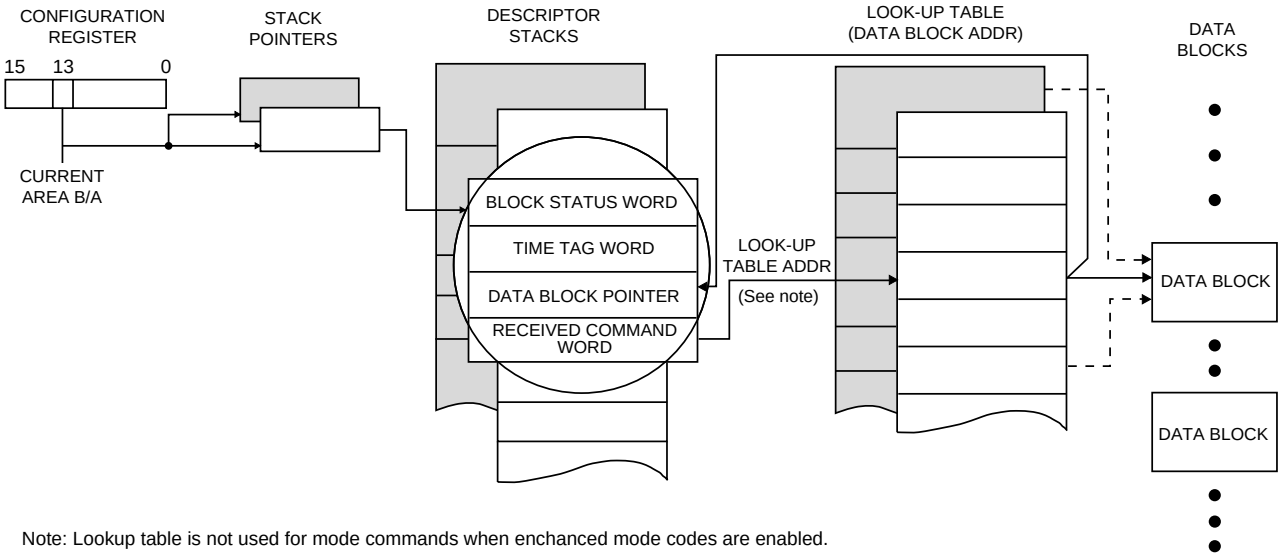
CIRCULAR BUFFER MODE

The operation of the Enhanced Mini-ACE's circular buffer RT memory management mode is illustrated in FIGURE 8. As in the single buffered and double buffered modes, the individual lookup table entries are initially loaded by the host processor. At the start of each message, the lookup table entry is stored in the third position of the respective message block descriptor in the descriptor stack area of RAM. Receive or transmit data words are transferred to (from) the circular buffer, starting at the location referenced by the lookup table pointer.

In general, the location after the last data word written or read (modulo the circular buffer size) during the message is written to the respective lookup table location during the end-of-message sequence. By so doing, data for the next message for the respective transmit, receive(/broadcast), or broadcast subaddress will be accessed from the next lower contiguous block of locations in the circular buffer.

For the case of a receive (or broadcast receive) message with a data word error, there is an option such that the lookup table pointer will only be updated following receipt of a **valid** message. That is, the pointer will **not** be updated following receipt of a message with an error in a data word. This allows failed messages in a bulk data transfer to be retried without disrupting the circular buffer data structure, and without intervention by the RT's host processor.

GLOBAL CIRCULAR BUFFER



Note: Lookup table is not used for mode commands when enchanced mode codes are enabled.

FIGURE 6. RT SINGLE BUFFERED MODE

Beyond the programmable choice of single buffer mode, double buffer mode, or circular buffer mode, programmable on an individual subaddress basis, the Enhanced Mini-ACE RT architecture provides an additional option, a variable sized **global** circular buffer. The Enhanced Mini-ACE RT allows for a mix of single buffered, double buffered, and individually circular buffered subaddresses, **along with** the use of the global double buffer for any arbitrary group of receive(/broadcast) or broadcast subaddresses.

In the global circular buffer mode, the data for **multiple** receive subaddresses is stored in the same circular buffer data structure. The size of the global circular buffer may be programmed for 128, 256, 512, 1024, 2048, 4096, or 8192 words, by means of bits 11, 10, and 9 of Configuration Register #6. As shown in TABLE 40, individual subaddresses may be mapped to the global circular buffer by means of their respective subaddress control words.

The pointer to the Global Circular Buffer will be stored in location 0101 (for Area A), or location 0105 (for Area B).

The global circular buffer option provides a highly efficient method for storing received message data. It allows for frequently used subaddresses to be mapped to individual data blocks, while also providing a method for asynchronously received messages to infrequently used subaddresses to be logged to a common area. Alternatively, the global circular buffer provides an efficient means for storing the received data words for **all** subaddresses. Under this method, all received data words are stored chronologically, regardless of subaddress.

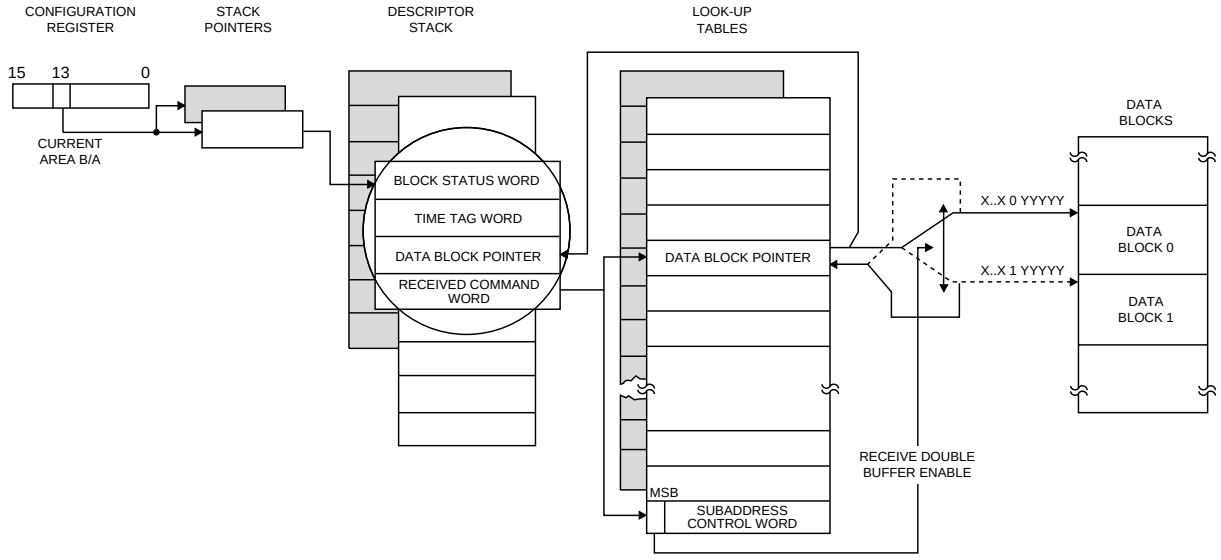
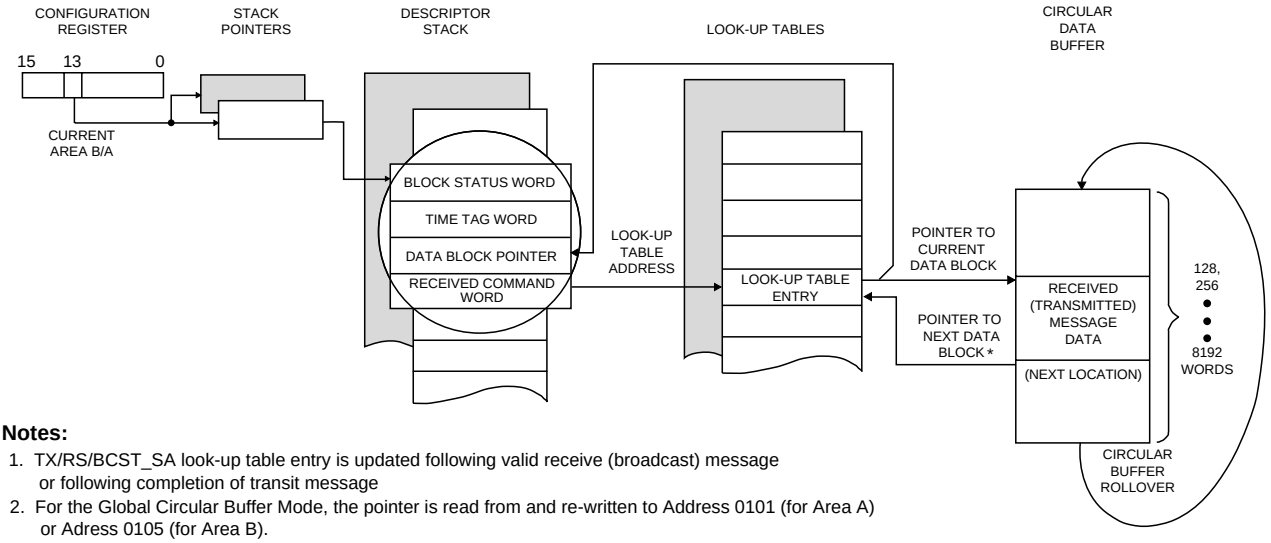


FIGURE 7. RT DOUBLE BUFFERED MODE



Notes:

1. TX/RS/BCST_SA look-up table entry is updated following valid receive (broadcast) message or following completion of transit message
2. For the Global Circular Buffer Mode, the pointer is read from and re-written to Address 0101 (for Area A) or Adress 0105 (for Area B).

FIGURE 8. RT CIRCULAR BUFFERED MODE

RT DESCRIPTOR STACK

The descriptor stack provides a chronology of all messages processed by the Enhanced Mini-ACE RT. Reference Figures 6, 7, and 8. Similar to BC mode, there is a four-word block descriptor in the Stack for each message processed. The four entries to each block descriptor are the Block Status Word, Time Tag Word, the pointer to the start of the message's data block, and the 16-bit received Command Word.

The RT Block Status Word includes indications of whether a particular message is ongoing or has been completed, what bus channel it was received on, indications of illegal commands, and flags denoting various message error conditions. For the double buffering, subaddress circular buffering, and global circular buffering modes, the data block pointer may be used for locating the data blocks for specific messages. Note that for mode code commands, there is an option to store the transmitted or received data word as the third word of the descriptor, in place of the data block pointer.

The Time Tag Word provides a 16-bit indication of relative time for individual messages. The resolution of the Enhanced Mini-ACE's time tag is programmable from among 2, 4, 8, 16, 32, or 64 µs/LSB. There is also a provision for using an external clock input for the time tag (consult factory). If enabled, there is a time tag rollover interrupt, which is issued when the value of the time tag rolls over from FFFF(hex) to 0. Other time tag options include the capabilities to clear the time tag register following receipt of a Synchronize (without data) mode command and/or to set the time tag following receipt of a Synchronize (with data) mode command. For that latter, there is an added option to filter the "set" capability based on the LSB of the received data word being equal to logic "0".

RT INTERRUPTS

The Enhanced Mini-ACE offers a great deal of flexibility in terms of RT interrupt processing. By means of the Enhanced Mini-ACE's two Interrupt Mask Registers, the RT may be programmed to issue interrupt requests for the following events/conditions: End-of-(every)Message, Message Error, Selected (transmit or receive) Subaddress, 100% Circular Buffer Rollover, 50% Circular Buffer Rollover, 100% Descriptor Stack Rollover, 50% Descriptor Stack Rollover, Selected Mode Code, Transmitter Timeout, Illegal Command, and Interrupt Status Queue Rollover.

Interrupts for 50% Rollovers of Stacks and Circular Buffers. The Enhanced Mini-ACE RT and Monitor are capable of issuing host interrupts when a subaddress circular buffer pointer or stack pointer crosses its mid-point boundary. For RT circular buffers, this is applicable for both transmit and receive subaddresses. Reference FIGURE 9. There are four interrupt mask and interrupt status register bits associated with the 50% rollover function:

(1) RT circular buffer;
(2) RT command (descriptor) stack;
(3) Monitor command (descriptor) stack; and
(4) Monitor data stack.

The 50% rollover interrupt is beneficial for performing bulk data transfers. For example, when using circular buffering for a particular receive subaddress, the 50% rollover interrupt will inform the host processor when the circular buffer is half full. At that time, the host may proceed to read the received data words in the upper half of the buffer, while the Enhanced Mini-ACE RT writes received data words to the lower half of the circular buffer. Later, when the RT issues a 100% circular buffer rollover interrupt, the host can proceed to read the received data from the lower half of the buffer, while the Enhanced Mini-ACE RT continues to write received data words to the upper half of the buffer.

Interrupt status queue. The Enhanced Mini-ACE RT, Monitor, and combined RT/Monitor modes include the capability for generating an interrupt status queue. As illustrated in Figure 10, this provides a chronological history of interrupt generating events and conditions. In addition to the Interrupt Mask Register, the Interrupt Status Queue provides additional filtering capability, such that only valid messages and/or only invalid messages may result in the creation of an entry to the Interrupt Status Queue. Queue entries for invalid and/or valid messages may be disabled by means of bits 8 and 7 of configuration register #6.

The interrupt status queue is 64 words deep, providing the capability to store entries for up to 32 messages. These events and conditions include both message-related and non-message related events. Note that the Interrupt Vector Queue Pointer Register will always point to the next location (modulo 64) following the last vector/pointer pair written by the Enhanced Mini-ACE RT.

The pointer to the Interrupt Status Queue is stored in the INTERRUPT VECTOR QUEUE POINTER REGISTER (register address 1F). This register must be initialized by the host, and is subsequently incremented by the RT message processor. The interrupt status queue is 64 words deep, providing the capability to store entries for up to 32 messages.

The queue rolls over at addresses of modulo 64. The events that result in queue entries include both message-related and non-message-related events. Note that the Interrupt Vector Queue Pointer Register will always point to the next location (modulo 64) **following** the last vector/pointer pair written by the Enhanced Mini-ACE RT, Monitor, or RT/Monitor.

Each event that causes an interrupt results in a two-word entry to be written to the queue. The first word of the entry is the interrupt vector. The vector indicates which interrupt event(s)/condition(s) caused the interrupt.

The interrupt events are classified into two categories: message interrupt events and non-message interrupt events. Message-based interrupt events include End-of-Message, Selected mode code, Format error, Subaddress control word interrupt, RT Circular buffer Rollover, Handshake failure, RT Command stack rollover, transmitter timeout, MT Data Stack rollover, MT Command Stack rollover, RT Command Stack 50% rollover, MT Data Stack 50% rollover, MT Command Stack 50% rollover, and RT Circular buffer 50% rollover. Non-message interrupt

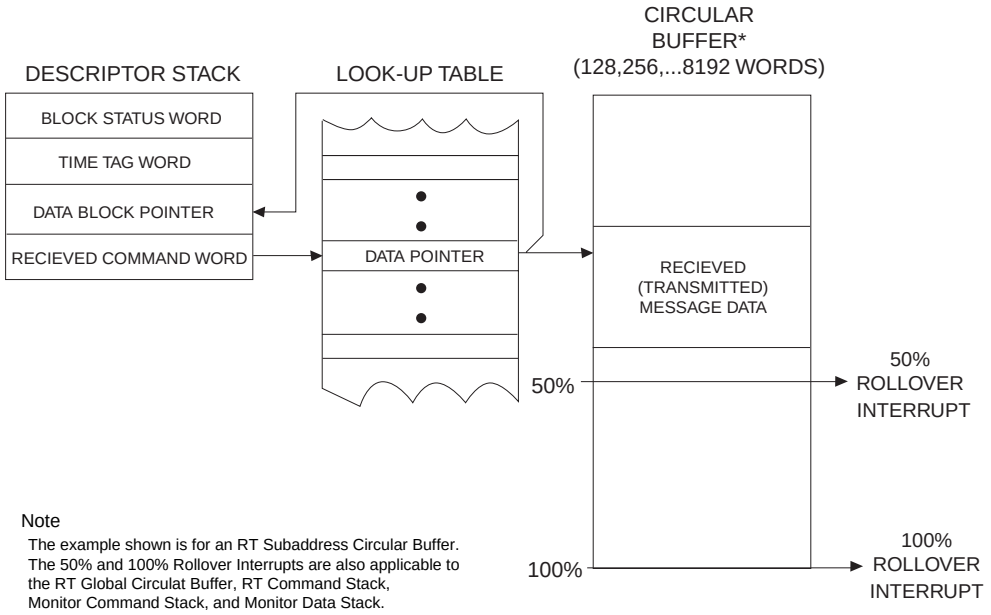


FIGURE 9. 50% and 100% ROLLOVER INTERRUPTS

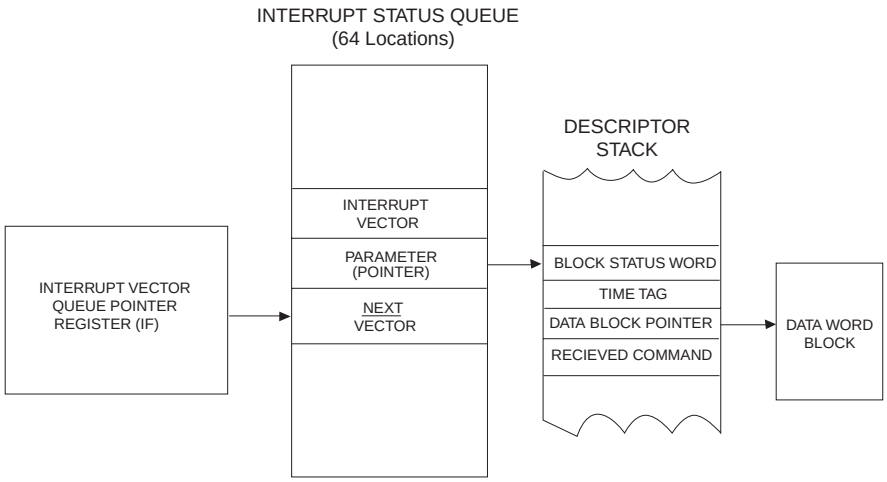


FIGURE 10. RT (and MONITOR) INTERRUPT STATUS QUEUE (shown for message Interrupt event)

events/conditions include time tag rollover, RT address parity error, RAM parity error, and BIT completed.

Bit 0 of the interrupt vector (interrupt status) word indicates whether the entry is for a message interrupt event (if bit 0 is logic "1") or a non-message interrupt event (if bit 0 is logic "0"). It is **not** possible for one entry on the queue to indicate both a message interrupt and a non-message interrupt.

As illustrated in FIGURE 10, for a message interrupt event, the parameter word is a pointer. The pointer will reference the first word of the RT or MT command stack descriptor (i.e., the Block Status Word).

For a RAM Parity Error non-message interrupt, the parameter will be the RAM address where the parity check failed. For the RT address Parity Error, Protocol Self-test Complete, and Time Tag rollover non-message interrupts, the parameter is not used; it will have a value of 0000.

If enabled, an INTERRUPT STATUS QUEUE ROLLOVER interrupt will be issued when the value of the queue pointer address rolls over at a 64-word address boundary.

RT COMMAND ILLEGALIZATION

The Enhanced Mini-ACE provides an internal mechanism for RT Command Word illegalizing. By means of a 256-word area in shared RAM, the host processor may designate that any message be illegalized, based on the command word $T/\overline{R}$ bit, subaddress, and word count/mode code fields. The Enhanced Mini-ACE illegalization scheme provides the maximum in flexibility, allowing any subset of the 4096 possible combinations of broadcast/own address, $T/\overline{R}$ bit, subaddress, and word count/mode code to be illegalized.

The address map of the Enhanced Mini-ACE's illegalizing table is illustrated in TABLE 41.

TABLE 41. ILLEGALIZATION TABLE MEMORY MAP

ADDRESS	DESCRIPTION
300	Brdcst / Rx, SA 0. MC15-0
301	Brdcst / RX,SA 0. MC31-16
302	Brdcst / Rx, SA 1. WC15-0
303	Brdcst / Rx, SA 1. WC31-16
• • •	• • •
33F	Brdcst / Rx, SA 31. MC31-16
340	Brdcst / Tx, SA 0. MC15-0
341	Brdcst / Tx, SA 1.MC31-16
342	Brdcst / Tx, SA 1. WC15-0
• • •	• • •
37D	Brdcst / Tx, SA 30. WC31-16
37E	Brdcst / Tx, SA 31. MC15-0
37F	Brdcst / Tx, SA 31. MC31-16
380	Own Addr / Rx, SA 0. MC15-0
381	Own Addr / Rx, SA 0. MC31-16
382	Own Addr / Rx, SA 1. WC15-0
383	Own Addr / Rx, SA 1. WC31-16
• • •	• • •
3BE	Own Addr / Rx, SA 31. MC15-0
3BF	Own Addr / Rx, SA 31. MC31-16
3C0	Own Addr / Tx, SA 0. MC15-0
3C1	Own Addr / Tx, SA 0. MC31-16
3C2	Own Addr / Tx, SA 1. WC15-0
3C3	Own Addr / Tx, SA 1. WC31-16
• • •	• • •
3FC	Own Addr / Tx, SA 30. WC15-0
3FD	Own Addr / Tx, SA 30. WC31-16
3FE	Own Addr / Tx, SA 31. MC15-0
3FF	Own Addr / Tx, SA 31. MC31-16

BUSY BIT

The Enhanced Mini-ACE RT provides two different methods for setting the Busy status word bit: (1) globally, by means of Configuration Register #1; or (2) on a T/R-bit/subaddress basis, by means of a RAM lookup table. If the host CPU asserts the $\overline{\text{BUSY}}$ bit to logic “0“ in Configuration Register #1, the Enhanced Mini-ACE RT will respond to **all** non-broadcast commands with the Busy bit set in its RT Status Word.

Alternatively, there is a Busy lookup table in the Enhanced Mini-ACE shared RAM. By means of this table, it is possible for the host processor to set the busy bit for any selectable subset of the 128 combinations of broadcast/own address, $T/\overline{R}$ bit, and subaddress.

If the busy bit is set for a transmit command, the Enhanced Mini-ACE RT will respond with the busy bit set in the status word, but will not transmit any data words. If the busy bit is set for a receive command, the RT will also respond with the busy status bit set. There are two programmable options regarding the reception of data words for a non-mode code receive command for which the RT is busy: (1) to transfer the received data words to shared RAM; or (2) to **not** transfer the data words to shared RAM.

RT ADDRESS

The Enhanced Mini-ACE offers several different options for designating the Remote Terminal address. These include the following: (1) hardwired, by means of the 5 RT ADDRESS inputs, and the RT ADDRESS PARITY input; (2) by means of the RT ADDRESS (and PARITY) inputs, but latched via hardware, on the rising edge of the RT_AD_LAT input signal; (3) input by means of the RT ADDRESS (and PARITY) inputs, but latched via host software; and (4) software programmable, by means of an internal register. In all four configurations, the RT address is readable by the host processor.

RT BUILT-IN-TEST (BIT) WORD

The bit map for the Enhanced Mini-ACE's internal RT Built-in-Test (BIT) Word is indicated in TABLE 42.

TABLE 42. RT BIT WORD

BIT	DESCRIPTION
15(MSB)	TRANSMITTER TIMEOUT
14	LOOP TEST FAILURE B
13	LOOP TEST FAILURE A
12	HANDSHAKE FAILURE
11	TRANSMITTER SHUTDOWN B
10	TRANSMITTER SHUTDOWN A
9	TERMINAL FLAG INHIBITED
8	BIT TEST FAILURE
7	HIGH WORD COUNT
6	LOW WORD COUNT
5	INCORRECT SYNC RECEIVED
4	PARITY / MANCHESTER ERROR RECEIVED
3	RT-to-RT GAP / SYNC ADDRESS ERROR
2	RT-to-RT NO RESPONSE ERROR
1	RT-to-RT 2ND COMMAND WORD ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

RT AUTO-BOOT OPTION

If utilized, the RT pin-programmable auto-boot option allows the Enhanced Mini-ACE RT to automatically initialize as an active remote terminal with the Busy status word bit set to logic "1" immediately following power turn-on. This is a useful feature for MIL-STD-1760 applications, in which the RT is required to be responding within 150 ms after power-up. This feature is available for versions of the Enhanced Mini-ACE with 4K words of RAM.

OTHER RT FEATURES.

The Enhanced Mini-ACE includes options for the Terminal flag status word bit to be set either under software control and/or automatically following a failure of the loopback self-test. Other software programmable RT options include software programmable RT status and RT BIT words, automatic clearing of the Service Request bit following receipt of a Transmit vector word mode command, options regarding Data Word transfers for the Busy and Message error (illegal) Status word bits, and options for the handling of 1553A and reserved mode codes.

MONITOR ARCHITECTURE

The Enhanced Mini-ACE includes three monitor modes:

(1) A Word Monitor mode.

(2) A selective message monitor mode.

(3) A combined RT/message monitor mode.

For new applications, it is recommended that the selective message monitor mode be used, rather than the word monitor mode. Besides providing monitor filtering based on RT address, T/$\overline{R}$ bit, and subaddress, the message monitor eliminates the need to determine the start and end of messages by software.

WORD MONITOR MODE

In the Word Monitor Terminal mode, the Enhanced Mini-ACE monitors both 1553 buses. After the software initialization and Monitor Start sequences, the Enhanced Mini-ACE stores all Command, Status, and Data Words received from both buses. For each word received from either bus, a pair of words is stored to the Enhanced Mini-ACE's shared RAM. The first word is the word received from the 1553 bus. The second word is the Monitor Identification (ID), or "Tag" word. The ID word contains information relating to bus channel, word validity, and inter-word time gaps. The data and ID words are stored in a circular buffer in the shared RAM address space.

WORD MONITOR MEMORY MAP

A typical word monitor memory map is illustrated in TABLE 43. TABLE 43 assumes a 64K address space for the Enhanced Mini-ACE's monitor. The Active Area Stack pointer provides the address where the first monitored word is stored. In the example, it is assumed that the Active Area Stack Pointer for Area A (location 0100) is initialized to 0000. The first received data word is stored in location 0000, the ID word for the first word is stored in location 0001, etc.

TABLE 43. TYPICAL WORD MONITOR MEMORY MAP

HEX ADDRESS	FUNCTION
0000	First Received 1553 Word
0001	First Identification Word
0002	Second Received 1553 Word
0003	Second Identification Word
0004	Third Received 1553 Word
005	Third Identification Word
• • •	• • •
0100	Stack Pointer (Fixed Location - gets overwritten)
• • • FFFF	• • Received 1553 Words and Identification Word • •

The current Monitor address is maintained by means of a counter register. This value may be read by the CPU by means of the Data Stack Address Register. It is important to note that when the counter reaches the Stack Pointer address of 0100 or 0104, the initial pointer value stored in this shared RAM location **will be overwritten** by the monitored data and ID Words. When the internal counter reaches an address of FFFF (or 0FFF, for an Enhanced Mini-ACE with 4K RAM), the counter rolls over to 0000.

WORD MONITOR TRIGGER

In the Word Monitor mode, there is a pattern recognition trigger and a pattern recognition interrupt. The 16-bit compare word for both the trigger and the interrupt is stored in the Monitor Trigger Word Register. The pattern recognition interrupt is enabled by setting the MT Pattern Trigger bit in Interrupt Mask Register #1. The pattern recognition trigger is enabled by setting the Trigger Enable bit in Configuration Register #1 and selecting either the Start-on-trigger or the Stop-on-trigger bit in Configuration Register #1.

The Word Monitor may also be started by means of a low-to-high transition on the EXT_TRIG input signal.

SELECTIVE MESSAGE MONITOR MODE

The Enhanced Mini-ACE Selective Message Monitor provides monitoring of 1553 messages with filtering based on RT address, T/$\overline{R}$ bit, and subaddress with no host processor intervention. By autonomously distinguishing between 1553 command and status words, the Message Monitor determines when messages begin and end, and stores the messages into RAM, based on a programmable filter of RT address, T/$\overline{R}$ bit, and subaddress.

The selective monitor may be configured as just a monitor, or as a **combined RT/Monitor.** In the combined RT/Monitor mode, the Enhanced Mini-ACE functions as an RT for one RT address (including broadcast messages), and as a selective message monitor for the other 30 RT addresses. The Enhanced Mini-ACE Message Monitor contains two stacks, a command stack and a data stack, that are independent from the RT command stack. The pointers for these stacks are located at fixed locations in RAM.

MONITOR SELECTION FUNCTION

Following receipt of a valid command word in Selective Monitor mode, the Enhanced Mini-ACE will reference the selective monitor lookup table to determine if the particular command is enabled. The address for this location in the table is determined by means of an offset based on the RT Address, T/$\overline{R}$ bit, and Subaddress bit 4 of the current command word, and concatenating it to the monitor lookup table base address of 0280 (hex). The bit location within this word is determined by subaddress bits 3-0 of the current command word.

If the specified bit in the lookup table is logic "0", the command is not enabled, and the Enhanced Mini-ACE will ignore this command. If this bit is logic "1", the command is enabled and the Enhanced Mini-ACE will create an entry in the monitor command descriptor stack (based on the monitor command stack pointer), and store the data and status words associated with the command into sequential locations in the monitor data stack. In addition, for an RT-to-RT transfer in which the receive command is selected, the second command word (the transmit command) is stored in the monitor data stack.

The address definition for the Selective Monitor Lookup TABLE is illustrated in TABLE 44.

TABLE 44. MONITOR SELECTION TABLE LOOKUP ADDRESS

BIT	DESCRIPTION
15(MSB)	Logic “0”
14	Logic “0”
13	Logic “0”
12	Logic “0”
11	Logic “0”
10	Logic “0”
9	Logic “1”
8	Logic “0”
7	Logic “1”
6	RTAD_4
5	RTAD_3
4	RTAD_2
3	RTAD_1
2	RTAD_0
1	TRANSMIT / $\overline{\text{RECEIVE}}$
0(LSB)	SUBADDRESS 4

SELECTIVE MESSAGE MONITOR MEMORY

ORGANIZATION

A typical memory map for the ACE in the Selective Message Monitor mode, assuming a 4K RAM space, is illustrated in TABLE 45. This mode of operation defines several fixed locations in the RAM. These locations are allocated in a way in which none of them overlap with the fixed RT locations. This allows for the combined RT/Selective Message Monitor mode.

The fixed memory map consists of two Monitor Command Stack Pointers (locations 102 and 106 hex), two Monitor Data Stack Pointers (locations 103 and 107 hex), and a Selective Message Monitor Lookup Table (locations 0280 through 02FF hex).

TABLE 45. TYPICAL SELECTIVE MESSAGE MONITOR MEMORY MAP (shown for 4K RAM for “Monitor only” mode)

ADDRESS (HEX)	DESCRIPTION
0000-0101	Not Used
0102	Monitor Command Stack Pointer A (fixed location)
0103	Monitor Data Stack Pointer A (fixed location)
0104-0105	Not Used
0106	Monitor Command Stack Pointer B (fixed location)
0107	Monitor Data Stack Pointer B (fixed location)
0108-027F	Not Used
0280-02FF	Selective Monitor Lookup Table (fixed location)
0300-03FF	Not Used
0400-07FF	Monitor Command Stack A
0800-0FFF	Monitor Data Stack A

For this example, the Monitor Command Stack size is assumed to be 1K words, and the Monitor Data Stack size is assumed to be 2K words.

FIGURE 11 illustrates the Selective Message Monitor operation. Upon receipt of a valid Command Word, the Enhanced Mini-ACE will reference the Selective Monitor Lookup Table to determine if the current command is enabled. If the current command is disabled, the Enhanced Mini-ACE monitor will ignore (and not store) the current message. If the command is enabled, the monitor will create an entry in the Monitor Command Stack at the address location referenced by the Monitor Command Stack Pointer, and an entry in the monitor data stack starting at the location referenced by the Monitor Data Stack Pointer.

The format of the information in the data stack depends on the format of the message that was processed. For example, for a BC-to-RT transfer (receive command), the monitor will store the command word in the monitor command descriptor stack, with the data words and the receiving RT's status word stored in the monitor data stack.

The size of the monitor command stack is programmable, with choices of 256, 1K, 4K, or 16K words. The monitor data stack size is programmable with choices of 512, 1K, 2K, 4K, 8K, 16K, 32K or 64K words.

Monitor Interrupts. Selective monitor interrupts may be issued for End-of-message and for conditions relating to the monitor command stack pointer and monitor data stack pointer. The latter, which are shown in FIGURE 9, include Command Stack 50% Rollover, Command Stack 100% Rollover, Data Stack 50% Rollover, and Data Stack 100% Rollover.

The 50% rollover interrupts may be used to inform the host processor when the command stack or data stack is half full. At that time, the host may proceed to read the received messages in the upper half of the respective stack, while the Enhanced Mini-ACE monitor writes messages to the lower half of the stack. Later, when the monitor issues a 100% stack rollover interrupt, the host can proceed to read the received data from the lower half of the stack, while the Enhanced Mini-ACE monitor continues to write received data words to the upper half of the stack.

INTERRUPT STATUS QUEUE

Like the Enhanced Mini-ACE RT, the Selective Monitor mode includes the capability for generating an interrupt status queue. As illustrated in FIGURE 10, this provides a chronological history of interrupt generating events. Besides the two Interrupt Mask Registers, the Interrupt Status Queue provides additional filtering capability, such that only valid messages and/or only invalid messages may result in entries to the Interrupt Status Queue. The interrupt status queue is 64 words deep, providing the capability to store entries for up to 32 monitored messages.

MISCELLANEOUS

CLOCK INPUT

The Enhanced Mini-ACE decoder is capable of operating from a 10, 12, 16, or 20 MHz clock input. Depending on the configuration of the specific model Enhanced Mini-ACE terminal, the selection of the clock input frequency may be chosen by one of either two methods. For all versions, the clock frequency may be specified by means of the host processor writing to Configuration Register #6. With the second method, which is applicable only for the versions incorporating 4K (but not 64K) words of internal RAM, the clock frequency may be specified by means of the input signals that are otherwise used as the A15 and A14 address lines.

ENCODER/DECODERS

For the selected clock frequency, there is internal logic to derive the necessary clocks for the Manchester encoder and decoders. For all clock frequencies, the decoders sample the receiver outputs on **both** edges of the input clock. By in effect doubling the decoders' sampling frequency, this serves to widen the tolerance to zero-crossing distortion, and reduce the bit error rate.

For interfacing to fiber optic transceivers (e.g., for MIL-STD-1773 applications), the decoders are capable of operating with single-ended, rather than double-ended, input signals. For applications involving the use of single-ended transceivers, it is suggested that you contact the factory at DDC regarding a transceiverless version of the Enhanced Mini-ACE.

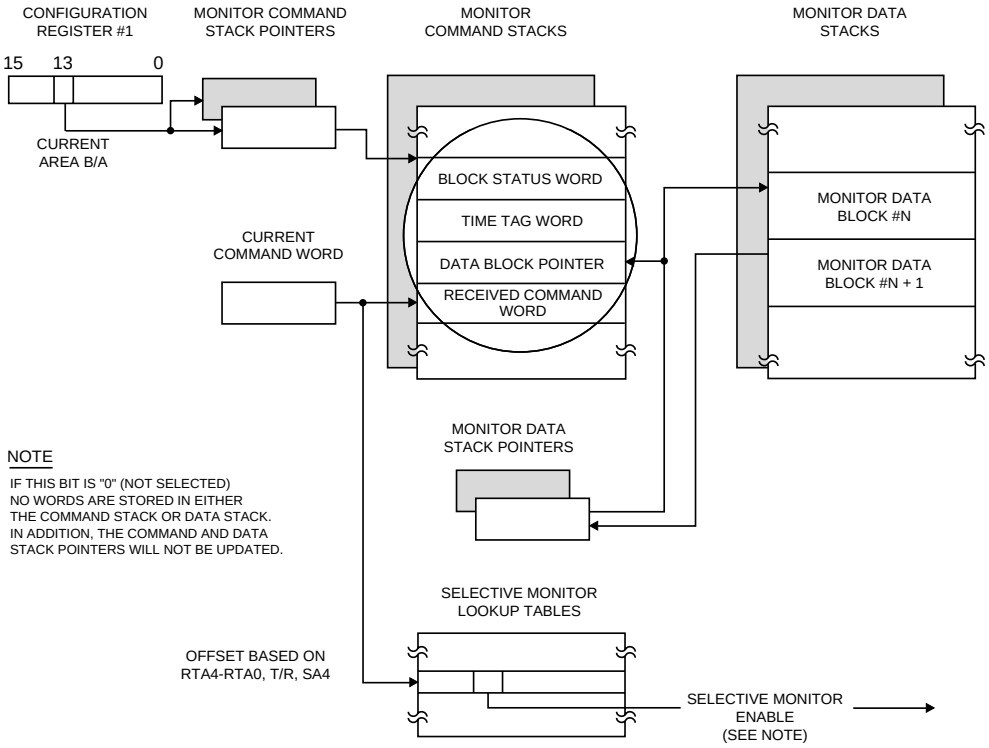


FIGURE 11. SELECTIVE MESSAGE MONITOR MEMORY MANAGEMENT

TIME TAG

The Enhanced Mini-ACE includes an internal read/writable Time Tag Register. This register is a CPU read/writable 16-bit counter with a programmable resolution of either 2, 4, 8, 16, 32, or 64 µs per LSB. Another option allows software controlled incrementing of the Time Tag Register. This supports self-test for the Time Tag Register. For each message processed, the value of the Time Tag Register is loaded into the second location of the respective descriptor stack entry ("TIME TAG WORD") for both the BC and RT modes.

The functionality involving the Time Tag Register that's compatible with ACE/Mini-ACE (Plus) includes: the capability to issue an interrupt request and set a bit in the Interrupt Status Register when the Time Tag Register rolls over FFFF to 0000; for RT mode, the capability to automatically clear the Time Tag Register following reception of a Synchronize (without data) mode command, or to load the Time Tag Register following a Synchronize (with data) mode command.

Additional time tag features supported by the Enhanced Mini-ACE include the capability for the BC to transmit the contents of the Time Tag Register as the data word for a Synchronize (with data) mode command; the capability for the RT to "filter" the data word for the Synchronize with data mode command, by only loading the Time Tag Register if the LSB of the received data word is "0"; an instruction enabling the BC Message Sequence Control engine to load the Time Tag Register with a specified value; and an instruction enabling the BC Message Sequence Control engine to write the value of the Time Tag Register to the General Purpose Queue.

INTERRUPTS

The Enhanced Mini-ACE series terminals provide many programmable options for interrupt generation and handling. The interrupt output pin ($\overline{\text{INT}}$) has three software programmable mode of operation: a pulse , a level output cleared under software control, or a level output automatically cleared following a read of the Interrupt Status Register (#1 or #2).

Individual interrupts are enabled by the two Interrupt Mask Registers. The host processor may determine the cause of the interrupt by reading the two Interrupt Status Registers, which provide the current state of interrupt events and conditions. The Interrupt Status Registers may be updated in two ways. In one interrupt handling mode, a particular bit in Interrupt Status Register #1 or #2 will be updated only if the event occurs **and** the corresponding bit in Interrupt Mask Register #1 or #2 is enabled. In the enhanced interrupt handling mode, a particular bit in the one of the Interrupt Status Registers will be updated if the event/condition occurs regardless of the value of the corresponding Interrupt Mask Register bit. In either case, the respective Interrupt Mask Register (#1 or #2) bit is used to enable an interrupt for a particular event/condition.

The Enhanced Mini-ACE supports all the interrupt events from ACE/Mini-ACE (Plus), including RAM Parity Error, Transmitter Timeout, BC/RT Command Stack Rollover, MT Command Stack and Data Stack Rollover, Handshake Error, BC Retry, RT Address Parity Error, Time Tag Rollover, RT Circular Buffer Rollover, BC Message, RT Subaddress, BC End-of-Frame, Format Error, BC Status Set, RT Mode Code, MT Trigger, and End-of-Message.

For the Enhanced Mini-ACE's Enhanced BC mode, there are four user-defined interrupt bits. The BC Message Sequence Control Engine includes an instruction enabling it to issue these interrupts at any time.

For RT and Monitor modes, the Enhanced Mini-ACE architecture include an Interrupt Status Queue. This provides a mechanism for logging messages that result in interrupt requests. Entries to the Interrupt Status Queue may be filtered such that only valid and/or invalid messages will result in entries on the queue.

The Enhanced Mini-ACE incorporates additional interrupt conditions beyond ACE/Mini-ACE (Plus), based on the addition of Interrupt Mask Register #2 and Interrupt Status Register #2. This is accomplished by chaining the two Interrupt Status Registers using the INTERRUPT CHAIN BIT (bit 0) in Interrupt Status Register #2 to indicate that an interrupt has occurred in Interrupt Status Register #1. Additional interrupts include "Self-Test Completed", masking bits for the Enhanced BC Control Interrupts, 50% Rollover interrupts for RT Command Stack, RT Circular Buffers, MT Command Stack, and MT Data Stack; BC Op Code Parity Error, (RT) Illegal Command, (BC) General Purpose Queue or (RT/MT) Interrupt Status Queue Rollover, Call Stack Pointer Register Error, BC Trap Op Code, and the four User-Defined interrupts for the Enhanced BC mode.

BUILT-IN TEST

A salient feature of the Enhanced Mini-ACE is its highly autonomous self-test capability. This includes both protocol and RAM self-tests. Either or both of these self-tests may be initiated by command(s) from the host processor.

The protocol test consists of a toggle test of 95% of the terminal's logic gates. The test includes a comprehensive test of all registers, Manchester encoder and decoders, transmitter failsafe timer, and protocol logic. This test is completed in approximately 32,000 clock cycles. That is, about 1.6 ms with a 20 MHz clock, 2.0 ms at 16 MHz, 2.7 ms at 12 MHz, and 3.2 ms at 10 MHz.

There is also a separate built-in test for the Enhanced Mini-ACE's 4K X 16 or 64K X 16 shared RAM. This test consists of writing and then reading/verifying the two walking patterns "data = address" and "data = address inverted". This test takes 10 clock cycles per word. For an Enhanced Mini-ACE with 4K words of RAM, this is about 2.0 ms with a 20 MHz clock, 2.6 ms at 16 MHz, 3.4 ms at 12 MHz, or 4.1 ms at 10 MHz. For an Enhanced Mini-ACE with 64K words of RAM, this test takes about 32.8 ms with a 20 MHz clock, 40.1 ms at 16 MHz, 54.6 ms at 12 MHz, or 65.6 ms at 10 MHz.

The Enhanced Mini-ACE built-in test may be initiated by a command from the host processor, via the START/REST REGISTER. For RT mode, this may include the host processor invoking self-test following receipt of an Initiate self-test mode command. The results of the self-test are host accessible by means of the BIT status register. For RT mode, the result of the self-test may

be communicated to the bus controller via bit 8 of the RT BIT word ("0" = pass, "1" = fail).

Assuming that the protocol self-test passes, all of the register and shared RAM locations will be restored to their state prior to the self-test, with the exception of the 60 RAM address locations 0342-037D and the TIME TAG REGISTER. Note that for RT mode, these locations map to the illegalization lookup table for "broadcast transmit subaddresses 1 through 30" (non-mode code subaddresses). Since MIL-STD-1553 does not define these as valid command words, this section of the illegalization lookup table is normally not used. The TIME TAG REGISTER will continue to increment during the self-test.

If there is a failure of the protocol self-test, it is possible to access information about the first failed vector. This may be done by means of the Enhanced Mini-ACE's upper registers (register addresses 32 through 63). Through these registers, it is possible to determine the self-test ROM address of the first failed vector, the expected response data pattern (from the ROM), the register or memory address, and the actual (incorrect) data value read from register or memory. The on-chip self-test ROM is 4K X 24.

Note that the RAM self-test is destructive. That is, following the RAM self-test, regardless of whether the test passes or fails, the shared RAM is **not** restored to its state prior to this test. Following a failed RAM self-test, the host may read the internal RAM to determine which location(s) failed the walking pattern test.

RAM PARITY

The BC/RT/MT version of the Enhanced Mini-ACE is available with options of 4K or 64K words of internal RAM. For the 64K option, the RAM is 17 bits wide. The 64K X 17 internal RAM allows for parity generation for RAM write accesses, and parity checking for RAM read accesses. This includes host RAM acesses, as well as acesses by the Enhanced Mini-ACE's internal logic. When the Enhanced Mini-ACE detects a RAM parity error, it reports it to the host processor by means of an interrupt and a register bit. Also, for the RT and Selective Message Monitor modes, the RAM address where a parity error was detected will be stored on the Interrupt Status Queue (if enabled).

RELOCATABLE MEMORY MANAGEMENT LOCATIONS

In the Enhanced Mini-ACE's default configuration, there is a *fixed* area of shared RAM addresses, 0000h-03FF, that is allocated for storage of the BC's or RT's pointers, counters, tables, and other "non-message" data structures. As a means of reducing the overall memory address space for using multiple Enhanced Mini-ACEs in a given system (e.g., for use with the DMA interface configuration), the Enhanced Mini-ACE allows this area of RAM to be relocated by means of 6 configuration register bits. To provide backwards compatibility to ACE and Mini-ACE, the default for this RAM area is 0000h-03FFh.

HOST PROCESSOR INTERFACE

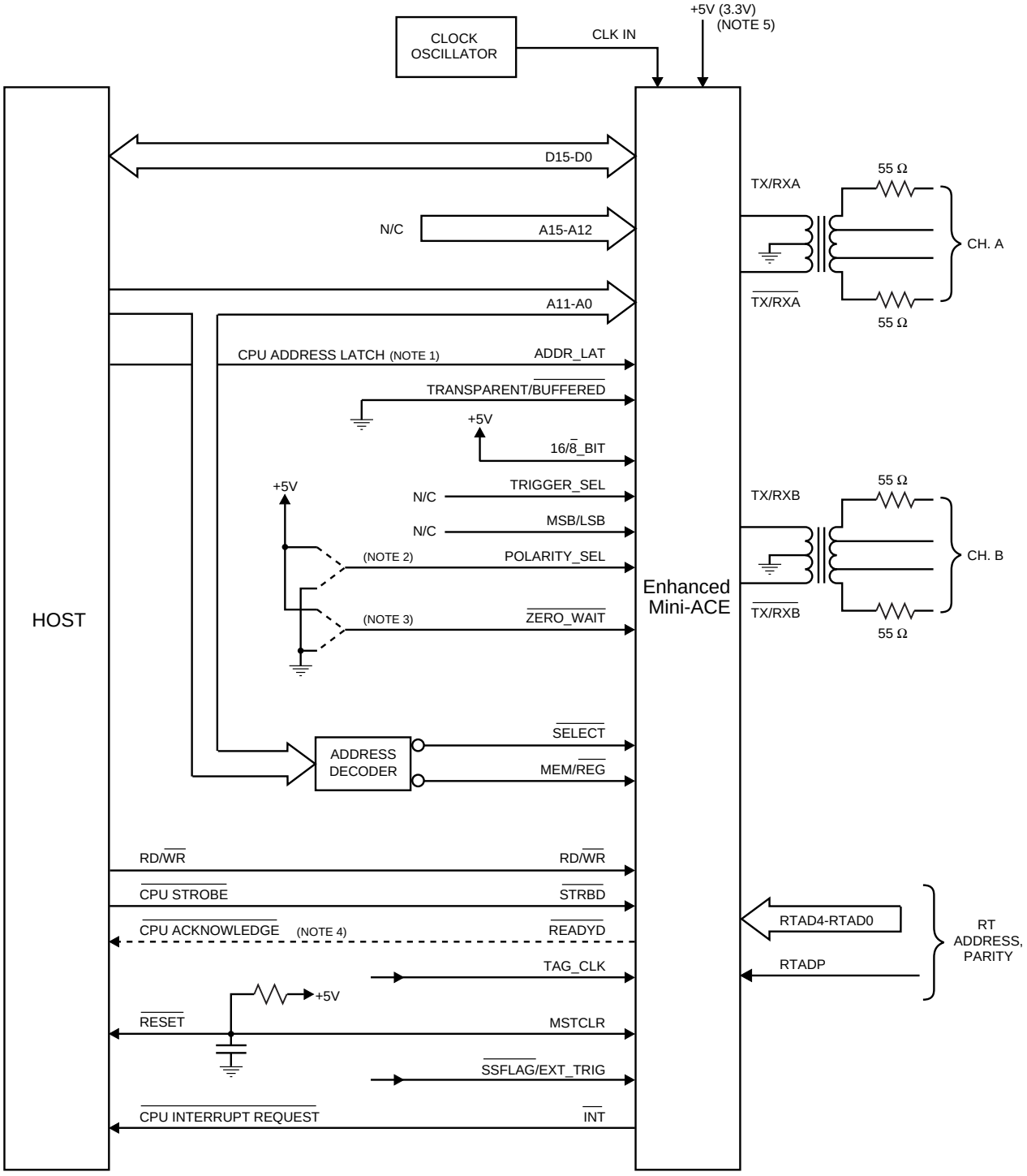
The Enhanced Mini-ACE supports a wide variety of processor interface configurations. These include shared RAM and DMA configurations, straightforward interfacing for 16-bit and 8-bit buses, support for both non-multiplexed and multiplexed address/data buses, non-zero wait mode for interfacing to a processor address/data buses, and zero wait mode for interfacing (for example) to microcontroller I/O ports. In addition, with respect to the ACE/Mini-ACE, the Enhanced Mini-ACE provides two major improvements: (1) reduced maximum host access time for shared RAM mode; and (2) increased maximum DMA grant time for the transparent/DMA mode.

The Enhanced Mini-ACE's maximum host holdoff time (time prior to the assertion of the $\overline{\text{READYD}}$ handshake signal) has been significantly reduced. For ACE/Mini-ACE, this maximum holdoff time is 10 internal word transfer cycles, resulting in an overall holdoff time of approximately 2.8 µs, using a 16 MHz clock. By comparison, using the Enhanced Mini-ACE's ENHANCED CPU ACCESS feature, this worst-case holdoff time is reduced significantly, to a single internal transfer cycle. For example, when operating the Enhanced Mini-ACE in its 16-bit buffered, non-zero wait configuration with a 16 MHz clock input, this results in a maximum overall host transfer cycle time of 632 ns for a read cycle, or 570 ns for a write cycle.

In addition, for using the ACE or Mini-ACE in the transparent/DMA configuration, the maximum request-to-grant time, which occurs prior to an RT start-of-message sequence, is 4.0 µs with a 16 MHz clock, or 3.5 µs with a 12 MHz clock. For the Enhanced Mini-ACE functioning as a MIL-STD-1553B RT, this time has been increased to 8.5 µs at 10 MHz, 10 µs at 16 MHz, 9 µs at 12 MHz, and 10.5 µs at 20MHz. This provides greater flexibility, particularly for systems in which a host has to arbitrate among multiple DMA requestors.

By far, the most commonly used processor interface configuration is the 16-bit buffered, non-zero wait mode. This configuration may be used to interface between 16-bit or 32-bit microprocessors and an Enhanced Mini-ACE. In this mode, only the Enhanced Mini-ACE's internal 4K or 64K words of internal RAM are used for storing 1553 message data and associated "housekeeping" functions. That is, in this configuration, the Enhanced Mini-ACE will never attempt to access memory on the host bus.

FIGURE 12 illustrates a generic connection diagram between a 16-bit (or 32-bit) microprocessor and an Enhanced Mini-ACE for the 16-bit buffered configuration, while Figures 13 and 14, and associated tables illustrate the processor read and write timing respectively.



NOTES:

1. CPU ADDRESS LATCH SIGNAL PROVIDED BY PROCESSORS WITH MULTIPLEXED ADDRESS/DATA BUSES. FOR PROCESSORS WITH NON-MULTIPLEXED ADDRESS AND DATA BUSSES, ADDR_LAT SHOULD BE CONNECTED TO +5V.
2. IF POLARITY_SEL = "1", RD/$\overline{WR}$ IS HIGH TO READ, LOW TO WRITE.
   IF POLARITY_SEL = "0", RD/$\overline{WR}$ IS LOW TO READ, HIGH TO WRITE.
3. $\overline{ZERO\_WAIT}$ SHOULD BE STRAPPED TO LOGIC "1" FOR NON-ZERO WAIT INTERFACE AND TO LOGIC "0" FOR ZERO WAIT INTERFACE.
4. $\overline{CPU\ ACKNOWLEDGE}$ PROCESSOR INPUT ONLY FOR NON-ZERO WAIT TYPE OF INTERFACE.
5. +3.3V POWER FOR BU-61743 / 61843 / 61864 **ONLY**

FIGURE 12. HOST PROCESSOR INTERFACE - 16-BIT BUFFERED CONFIGURATION

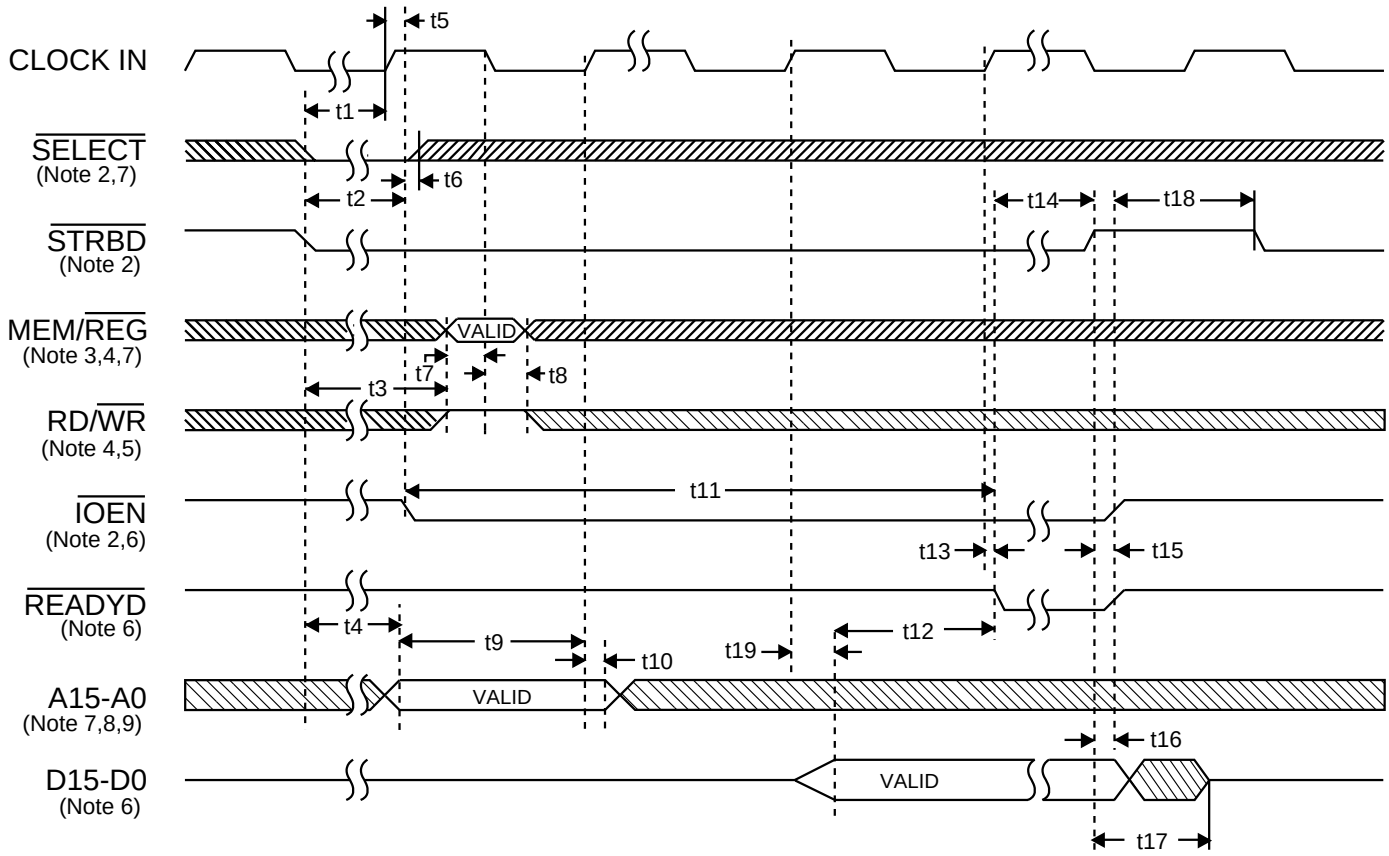


FIGURE 13. CPU READING RAM / REGISTER (16-BIT BUFFERED, NONZERO WAIT)

NOTES:

1. For the 16-bit buffered nonzero wait configuration, TRANSPARENT/$\overline{\text{BUFFERED}}$ must be connected to logic "0". $\overline{\text{ZERO WAIT}}$ and $\overline{\text{DTREQ}}$/16/$\overline{8}$ must be connected to logic "1". The inputs TRIGGER_SEL and MSB/LSB may be connected to either +5V or ground.
2. $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ may be tied together. $\overline{\text{IOEN}}$ goes low on the first rising CLK edge when $\overline{\text{SELECT}}$ • $\overline{\text{STRBD}}$ is sampled low (satisfying t1) and the Enhanced Mini-ACE's protocol/memory management logic is not accessing the internal RAM. When this occurs, $\overline{\text{IOEN}}$ goes low, starting the transfer cycle. After $\overline{\text{IOEN}}$ goes low, $\overline{\text{SELECT}}$ may be released high.
3. MEM/$\overline{\text{REG}}$ must be presented high for memory access, low for register access.
4. MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ are buffered transparently until the first falling edge of CLK after $\overline{\text{IOEN}}$ goes low. After this CLK edge, MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ become latched internally.
5. The logic sense for RD/$\overline{\text{WR}}$ in the diagram assumes that POLARITY_SEL is connected to logic "1." If POLARITY_SEL is connected to logic "0," RD/$\overline{\text{WR}}$ must be asserted low to read.
6. The timing for $\overline{\text{IOEN}}$, $\overline{\text{READYD}}$ and D15-D0 assumes a 50 pf load. For loading above 50 pf, the validity of $\overline{\text{IOEN}}$, $\overline{\text{READYD}}$, and D15-D0 is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.
7. The timing for A15-A0, MEM/$\overline{\text{REG}}$ and $\overline{\text{SELECT}}$ assumes that ADDR-LAT is connected to logic "1." Refer to Address Latch timing for additional details.
8. The address bus A15-A0 is internally buffered transparently until the first rising edge of CLK after $\overline{\text{IOEN}}$ goes low. After this CLK edge, A15-A0 become latched internally.
9. Setup time given for use in worst case timing calculations. None of the Enhanced Mini-ACE input signals are required to be synchronized to the system clock. When $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ do not meet the setup time of t1, but occur during the setup window of an internal flip-flop, an additional clock cycle will be inserted between the falling clock edge that latches MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ and the rising clock edge that latches the Address (A15-A0). When this occurs, the delay from $\overline{\text{IOEN}}$ falling to $\overline{\text{READYD}}$ falling (t11) increases by one clock cycle and the address hold time (t10) must be increased be one clock cycle.

TABLE FOR FIGURE 13. CPU READING RAM OR REGISTERS (SHOWN FOR 16-BIT, BUFFERED, NONZERO WAIT MODE)									
REF	DESCRIPTION	NOTES	5V LOGIC			3.3V LOGIC			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t1	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low setup time prior to clock rising edge	2, 9	10			15			ns
t2	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low to $\overline{\text{IOEN}}$ low (uncontended access @ 20 MHz)	2, 6			100			105	ns
	(contended access, with ENHANCED CPU SELECT = “0” @ 20 MHz)	2, 6			2.2			2.2	µs
	(contended access, with ENHANCED CPU SELECT = “1” @ 20 MHz)	2, 6			350			355	ns
	(uncontended access @ 16 MHz)	2, 6			112			117	ns
	(contended access, with ENHANCED CPU SELECT = “0” @ 16 MHz)	2, 6			2.8			2.8	µs
	(contended acces, with ENHANCED CPU SELECT = “1” s @ 16 MHz)	2, 6			425			430	ns
	(uncontended access @ 12 MHz)	2, 6			133			138	ns
	(contended access, with ENHANCED CPU SELECT = “0” @ 12 MHz)	2, 6			3.7			3.7	µs
	(contended access, with ENHANCED CPU SELECT = “1” @ 12 MHz)	2, 6			550			555	ns
	(uncontended access @ 10 MHz)	2, 6			150			155	ns
	(contended access, with ENHANCED CPU SELECT = “0” @ 10 MHz)	2, 6			4.4			4.4	µs
	(contended access, with ENHANCED CPU SELECT = “1” @ 10 MHz)	2, 6			650			655	ns
t3	Time for MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ to become valid following $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low(@ 20 MHz)	3, 4, 5, 7			15			10	ns
	@ 16 MHz	3, 4, 5, 7			21			16	ns
	@ 12 MHz	3, 4, 5, 7			32			27	ns
	@ 10 MHz	3, 4, 5, 7			40			35	ns
t4	Time for Address to become valid following $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low (@ 20 MHz)				17			12	ns
	@ 16 MHz				30			25	ns
	@ 12 MHz				50			45	ns
	@ 10 MHz				67			62	ns
t5	CLOCK IN rising edge delay to $\overline{\text{IOEN}}$ falling edge	6			40			40	ns
t6	$\overline{\text{SELECT}}$ hold time following $\overline{\text{IOEN}}$ falling	2	0			0			ns
t7	MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$ setup time prior to CLOCK IN falling edge	3, 4, 5, 7	10			15			ns
t8	MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$ hold time following CLOCK IN falling edge	3, 4, 5, 7	30			30			ns
t9	Address valid setup time prior to CLOCK IN rising edge	7, 8	30			35			ns
t10	Address hold time following CLOCK IN rising edge	7, 8, 9	30			30			ns
t11	$\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling (@ 20 MHz)	6, 9	135	150	165	135	150	165	ns
	@ 16 MHz	6, 9	170	187.5	205	170	187.5	205	ns
	@ 12 MHz	6, 9	235	250	265	235	250	265	ns
	@ 10 MHz	6, 9	285	300	315	285	300	315	ns
t12	Output Data valid prior to $\overline{\text{READYD}}$ falling (@ 20 MHz)	6	21			11			ns
	@ 16 MHz	6	33			23			ns
	@ 12 MHz	6	54			44			ns
	@ 10 MHz	6	71			61			ns
t13	CLOCK IN rising edge delay to $\overline{\text{READYD}}$ falling	6			40			40	ns
t14	$\overline{\text{READYD}}$ falling to $\overline{\text{STRBD}}$ rising release time				∞			∞	ns
t15	$\overline{\text{STRBD}}$ rising edge delay to $\overline{\text{IOEN}}$ rising edge and $\overline{\text{READYD}}$ rising edge	6			30			40	ns
t16	Output Data hold time following $\overline{\text{STRBD}}$ rising edge		0			0			ns
t17	$\overline{\text{STRBD}}$ rising delay to output data tri-state				40			40	ns
t18	$\overline{\text{STRBD}}$ high hold time from $\overline{\text{READYD}}$ rising		0			0			ns
t19	CLOCK IN rising edge delay to output data valid				40			40	ns

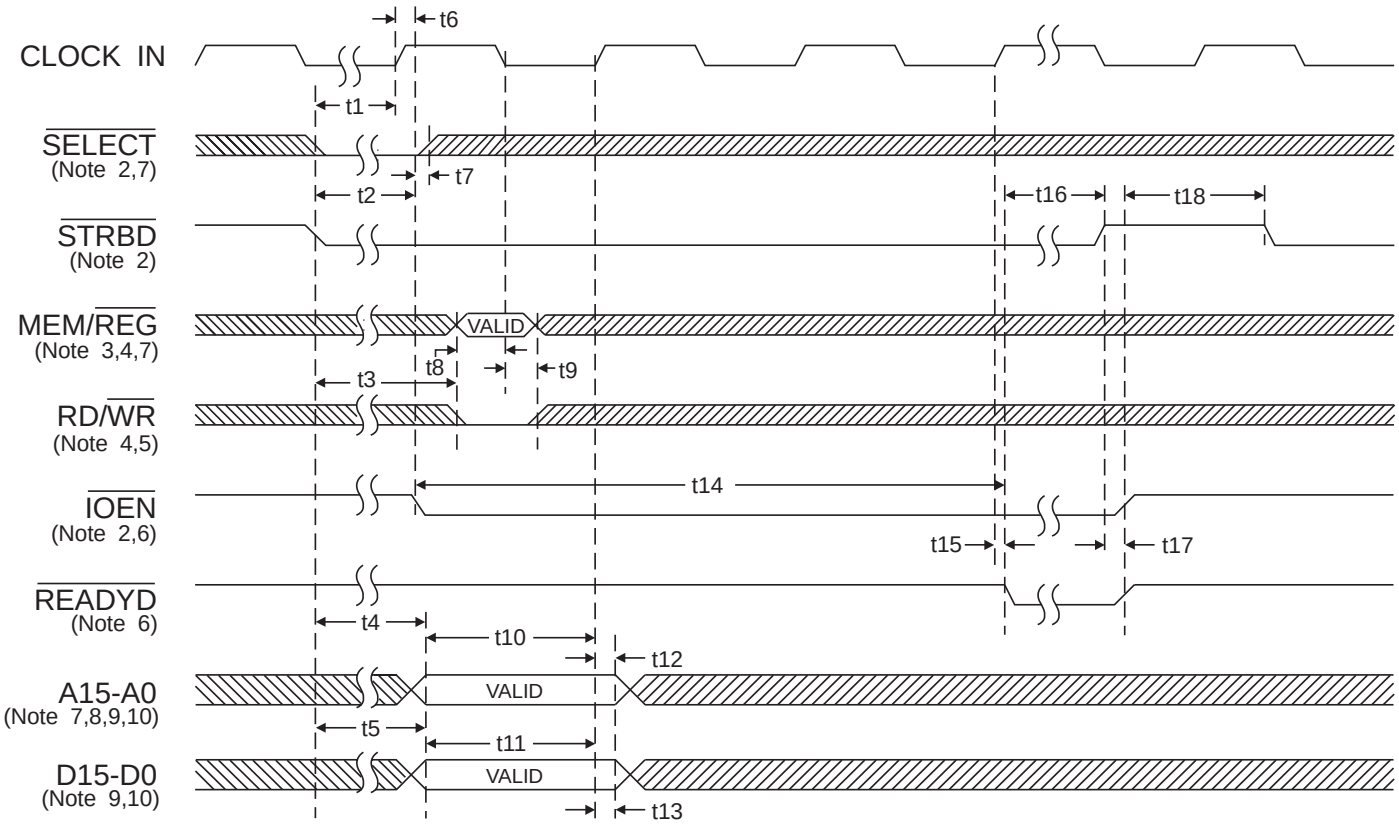


FIGURE 14. CPU WRITING RAM / REGISTER (16-BIT BUFFERED, NONZERO WAIT)

NOTES:

1. For the 16-bit buffered nonzero wait configuration TRANSPARENT/$\overline{\text{BUFFERED}}$ must be connected to logic "0", $\overline{\text{ZERO WAIT}}$ and $\overline{\text{DTREQ}}$/16/8 must be connected to logic "1". The inputs TRIGGER_SEL and MSB/LSB may be connected to either +5V or ground.
2. $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ may be tied together. $\overline{\text{IOEN}}$ goes low on the first rising CLK edge when $\overline{\text{SELECT}}$ • $\overline{\text{STRBD}}$ is sampled low (satisfying t1) and the Enhanced Mini-ACE's protocol/memory management logic is not accessing the internal RAM. When this occurs, $\overline{\text{IOEN}}$ goes low, starting the transfer cycle. After $\overline{\text{IOEN}}$ goes low, $\overline{\text{SELECT}}$ may be released high.
3. MEM/$\overline{\text{REG}}$ must be presented high for memory access, low for register access.
4. MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ are buffered transparently until the first falling edge of CLK after $\overline{\text{IOEN}}$ goes low. After this CLK edge, MEM/$\overline{\text{REG}}$ and RD/WR become latched internally.
5. The logic sense for RD/$\overline{\text{WR}}$ in the diagram assumes that POLARITY_SEL is connected to logic "1." If POLARITY_SEL is connected to logic "0," RD/WR must be asserted high to write.
6. The timing for the $\overline{\text{IOEN}}$ and $\overline{\text{READYD}}$ outputs assumes a 50 pf load. For loading above 50 pf, the validity of $\overline{\text{IOEN}}$ and $\overline{\text{READYD}}$ is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.
7. The timing for A15-A0, MEM/$\overline{\text{REG}}$, and $\overline{\text{SELECT}}$ assumes that ADDR-LAT is connected to logic "1." Refer to Address Latch timing for additional details.
9. The address bus A15-A0 and data bus D15-D0 are internally buffered transparently until the first rising edge of CLK after $\overline{\text{IOEN}}$ goes low. After this CLK edge, A15-A0 and D15-D0 become latched internally.
10. Setup time given for use in worst case timing calculations. None of the Enhanced Mini-ACE input signals are required to be synchronized to the system clock. When $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ do not meet the setup time of t1, but occur during the setup time of an internal flip-flop, an additional clock cycle may be inserted between the falling clock edge that latches MEM/$\overline{\text{REG}}$ and RD/$\overline{\text{WR}}$ and the rising clock edge that latches the address (A15-A0) and data (D15-D0). When this occurs, the delay from $\overline{\text{IOEN}}$ falling to $\overline{\text{READYD}}$ falling (t14) increases by one clock cycle and the address and data hold time (t12 and t13) must be increased by one clock.

TABLE FOR FIGURE 14. CPU WRITING RAM OR REGISTERS (SHOWN FOR 16-BIT, BUFFERED, NONZERO WAIT MODE)									
REF	DESCRIPTION	NOTES	5V LOGIC			3.3V LOGIC			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t1	SELECT and STRBD low setup time prior to clock rising edge	2, 10	10			15			ns
t2	SELECT and STRBD low to IOEN low (uncontended access @ 20 MHz)	2, 6			100			105	ns
	(contended access, with ENHANCED CPU SELECT = “0” @ 20 MHz)	2, 6			2.2			2.2	µs
	(contended access, with ENHANCED CPU SELECT = “1” @ 20 MHz)	2, 6			350			355	ns
	(uncontended access @ 16 MHz)	2, 6			112			117	ns
	(contended access, with ENHANCED CPU SELECT = “0” @ 16 MHz)	2, 6			2.8			2.8	µs
	(contended acces, with ENHANCED CPU SELECT = “1” @ 16 MHz)	2, 6			425			430	ns
	(uncontended access @ 12 MHz)	2, 6			133			138	ns
	(contended access, with ENHANCED CPU SELECT = “0” @ 12 MHz)	2, 6			3.7			3.7	µs
	(contended access, with ENHANCED CPU SELECT = “1” @ 12 MHz)	2, 6			550			555	ns
	(uncontended access @ 10 MHz)	2, 6			150			155	ns
	(contended access, with ENHANCED CPU SELECT = “0” @ 10 MHz)	2, 6			4.4			4.4	µs
	(contended access, with ENHANCED CPU SELECT = “1” @ 10 MHz)	2, 6			650			655	ns
t3	Tme for MEM/REG and RD/WR to become valid following SELECT and STRBD low(@ 20 MHz)	3, 4, 5, 7			15			10	ns
	@ 16 MHz	3, 4, 5, 7			21			16	ns
	@ 12 MHz	3, 4, 5, 7			32			27	ns
	@ 10 MHz	3, 4, 5, 7			40			35	ns
t4	Time for Address to become valid following SELECT and STRBD low (@ 20 MHz)				17			12	ns
	@ 16 MHz				30			25	ns
	@ 12 MHz				50			45	ns
	@ 10 MHz				67			62	ns
t5	Time for data to become valid following SELECT and STRBD low (@ 20 MHz)				37			32	ns
	@ 16 MHz				50			45	ns
	@ 12 MHz				70			65	ns
	@ 10 MHz				87			82	ns
t6	CLOCK IN rising edge delay to IOEN falling edge	6			40			40	ns
t7	SELECT hold time following IOEN falling	2	0			0			ns
t8	MEM/REG, RD/WR setup time prior to CLOCK IN falling edge	3, 4, 5, 7	10			15			ns
t9	MEM/REG, RD/WR setup time following CLOCK IN falling edge	3, 4, 5, 7	30			35			ns
t10	Address valid setup time prior to CLOCK IN rising edge	7, 8	30			35			ns
t11	Data valid setup time prior to CLOCK IN rising edge		10			15			ns
t12	Address valid hold time prior to CLOCK IN rising edge	7, 8, 9	30			30			ns
t13	Data valid hold time following CLOCK IN rising edge	9	10			15			ns
t14	IOEN falling delay to READYD falling @ 20 MHz	6, 9	85	100	115	85	100	115	ns
	@ 16 MHz	6, 9	110	125	140	110	125	140	ns
	@ 12 MHz	6, 9	152	167	182	152	167	182	ns
	@ 10 MHz	6, 9	185	200	215	185	200	215	ns
t15	CLOCK IN rising edge delay to READYD falling	6			40			40	ns
t16	READYD falling to STRBD rising release time				∞			∞	ns
t17	STRBD rising delay to IOEN rising edge and READYD rising edge	6			30			40	ns
t18	STRBD high hold time from READYD rising		0			0			ns

INTERFACE TO MIL-STD-1553 BUS

FIGURE 15 illustrates the interface between the various versions of the Enhanced Mini-ACE series and a MIL-STD-1553 bus. Connections for both direct (short stub) and transformer (long stub) coupling, as well as the nominal peak-to-peak voltage levels at various points (when transmitting), are indicated in the diagram.

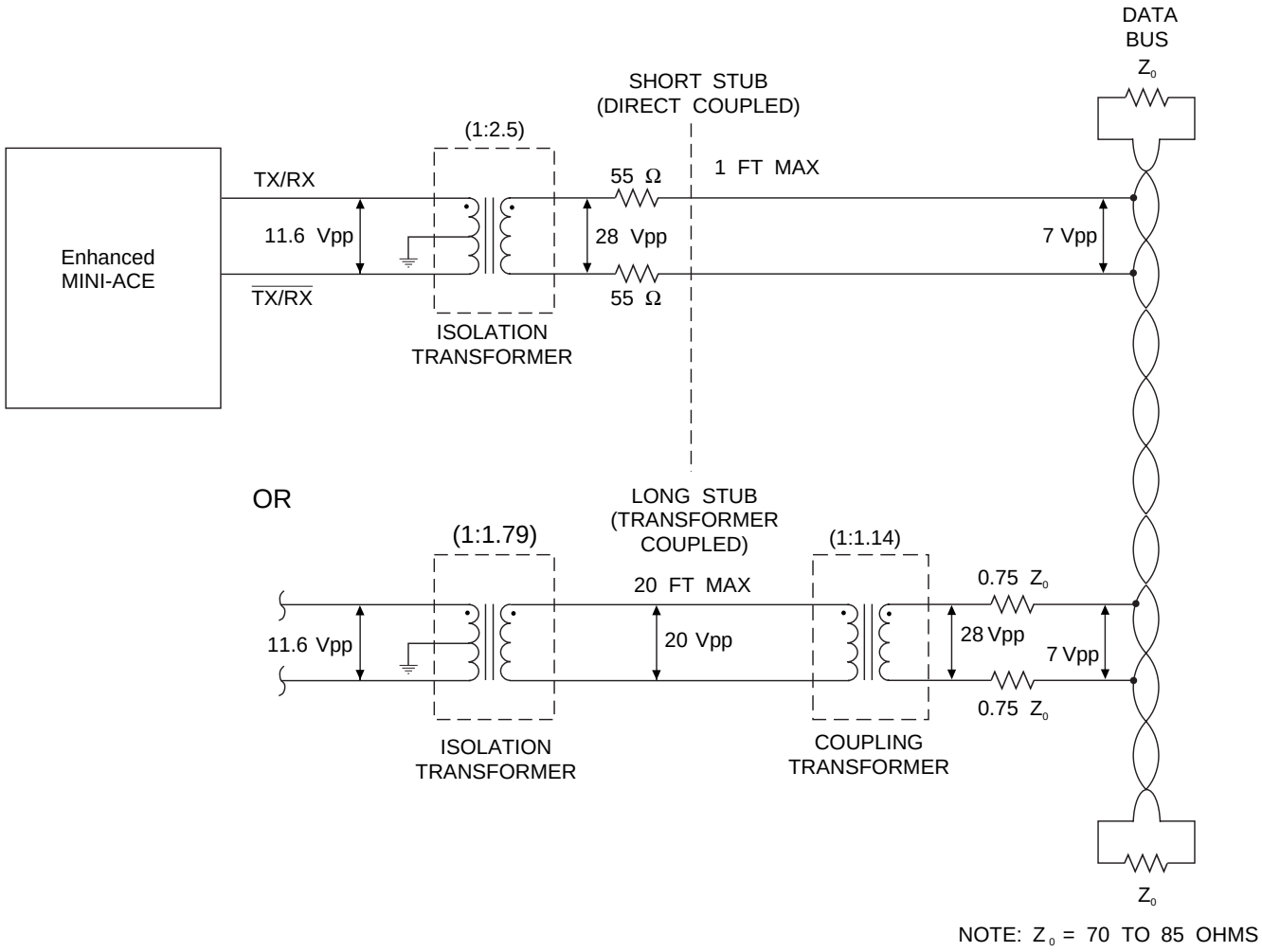


FIGURE 15. ENHANCED MINI-ACE INTERFACE TO MIL-STD-1553 BUS

TRANSFORMERS

In selecting isolation transformers to be used with the Enhanced Mini-ACE, there is a limitation on the maximum amount of leakage inductance. If this limit is exceeded, the transmitter rise and fall times may increase, possibly causing the bus amplitude to fall below the minimum level required by MIL-STD-1553. In addition, an excessive leakage imbalance may result in a transformer dynamic offset that exceeds 1553 specifications.

The maximum allowable leakage inductance is 6.0 µH, and is measured as follows:
The side of the transformer that connects to the Enhanced Mini-ACE is defined as the "primary" winding. If one side of the primary is shorted to the primary center-tap, the inductance should be measured across the "secondary" (stub side) winding. This inductance must be less tha 6.0 µH. Similarly, if the other side of the primary is shorted to the primary center-tap, the inductance measured accross the "secondary" (stub side) winding must also be less than 6.0 µH.

The difference between these two measurements is the "differential" leakage inductance. This value must be less than 1.0 µH.

Beta Transformer Technology Corporation (BTTC), a subsidiary of DDC, manufactures transformers in a variety of mechanical configurations with the required turns ratios of 1:2.5 direct coupled, and 1:1.79 transformer coupled. TABLE 46 provides a listing of many of these transformers.

For further information, contact BTTC at 631-244-7393 or at www.bttc-beta.com.

NOTES:

1. For the BU-6XXXXX**4** versions of the Enhanced Mini-ACE, which include the McAir-compatible transceivers, **only** the B-3818 or B-3819 transformers (shown in **bold** in the table) may be used.

2. For the BU-6XXXXX3 versions of the Enhanced Mini-ACE with -1553B transceivers, **any** of the transformers listed in the table may be used.

TABLE 46. BTTC TRANSFORMERS FOR USE WITH ENHANCED MINI-ACE

TRANSFORMER CONFIGURATION	BTTC PART NO.
Single epoxy transformer, through-hole, 0.625 X 0.625, 0.250" max height	B-3226
Single epoxy transformer, through-hole, 0.625 X 0.625, 0.220" max height. May be used with BU-6XXXXX4 versions of the Enhanced Mini-ACE.	**B-3818**
Single epoxy transformer, flat pack, 0.625" X 0.625", 0.275" max height	B-3231
Single epoxy transformer, surface mount, 0.625" X 0.625", 0.275" max height	B-3227
Single epoxy transformer, surface mount, hi-temp solder, 0.625" X 0.625", 0.220" max height. May be used with BU-6XXXXX4 versions of the Enhanced Mini-ACE.B-3819	**B-3819**
Single epoxy transformer, flat pack, 0.625" X 0.625", 0.150" max height	LPB-5014
Single epoxy transformer, surface mount, 0.625" X 0.625", 0.150" max height	LPB-5015
Dual epoxy transformer, twin stacked, 0.625" X 0.625", 0.280" max height	TST-9007
Dual epoxy transformer, twin stacked, surface mount, 0.625" X 0.625", 0.280" max height	TST-9017
Dual epoxy transformer, twin stacked, flat pack, 0.625" X 0.625", 0.280" max height	TST-9027
Dual epoxy transformer, side by side, through-hole, 0.930" X 0.630", 0.155 max height	B-3300
Dual epoxy transformer, side by side, flat pack, 0.930" X 0.630", 0.155 max height	B-3261
Dual epoxy transformer, side by side, surface mount, 0.930" X 0.630", 0.155 max height	B-3310
Single metal transformer, hermetically sealed, flat pack, 0.630" X 0.630", 0.175" max height	HLP-6014
Single metal transformer, hermetically sealed, surface mount, 0.630" X 0.630", 0.175" max height	HLP-6015

TABLE 47. SIGNAL DESCRIPTIONS BY FUNCTIONAL GROUPS

POWER AND GROUND			
SIGNAL NAME	**BU-61864(5) (64K RAM)**	**BU-61843(5) / 61743(5) (4KK RAM)**	**DESCRIPTION**
	PIN	**PIN**	
+5V Vcc CH A	72	72	Channel A transceiver power.
+5V Vcc CH B	20	20	Channel B transceiver power.
+5V / +3.3V Logic	37	37	Logic power. For BU-61864/61843/61743, this pin must be connected to **+3.3V**. For BU-61865/61845/61745, this pin must be connected to **+5V**.
+5V RAM	26	-	For BU-61864 or BU-61865, this pin must be connected to +5V. **Note that for BU-6184X/6174X, this pin assumes the function UPADDREN.**
GROUND	17	17	Ground.
	18	18	
	19	19	
	65	65	
	67	67	

1553 ISOLATION TRANSFORMER INTERFACE (4)		
SIGNAL NAME	**PIN**	**DESCRIPTION**
TX/RX-A (I/O)	5	Analog Transmit/Receive Input/Outputs. Connect directly to 1553 isolation transformers.
$\overline{\text{TX/RX-A}}$ (I/O)	7	
TX/RX-B (I/O)	13	
$\overline{\text{TX/RX-B}}$ (I/O)	16	

DATA BUS (16)		
SIGNAL NAME	**PIN**	**DESCRIPTION**
D15 (MSB)	53	16-bit bi-directional data bus. This bus interfaces the host processor to the Enhanced Mini-ACE's internal registers and internal RAM. In addition, in transparent mode, this bus allows data transfers to take place between the internal protocol/memory management logic and up to 64K x 16 of external RAM. Most of the time, the outputs for D15 through D0 are in the high impedance state. They drive outward in the buffered or transparent mode when the host CPU reads the internal RAM or registers. Also, in the transparent mode, D15-D0 will drive outward (towards the host) when the protocol/management logic is accessing (either reading or writing) internal RAM, or writing to external RAM. In the transparent mode, D15-D0 drives inward when the CPU writes internal registers or RAM, or when the protocol/memory management logic reads external RAM.
D14	50	
D13	48	
D12	49	
D11	52	
D10	54	
D9	51	
D8	46	
D7	47	
D6	36	
D5	45	
D4	39	
D3	44	
D2	43	
D1	38	
D0 (LSB)	42	

<table>
<tr><th colspan="4">PROCESSOR ADDRESS BUS</th></tr>
<tr><th colspan="2">SIGNAL NAME</th><th rowspan="2">PIN</th><th rowspan="2">DESCRIPTION</th></tr>
<tr><th>BU-61864(5)
(64K RAM)</th><th>BU-61843(5) /
61743(5)
(4KK RAM)</th></tr>
<tr><td>A15</td><td>A15 / CLK_SEL_1</td><td>66</td><td>For BU-61864(5) (64K RAM version), this signal is always configured as address line A15 (MSB). Refer to the description for A11-A0 below.

For BU-61843(5)/61743(5) (4K RAM version), if UPADDREN is connected to logic "1", this signal operates as address line A15.

For BU-61843(5)/61743(5) (4K RAM version), if UPADDREN is connected to logic "0", this signal operates as CLK_SEL_1. In this case, A15/CLK_SEL_1 and A14/CLK_SEL_0 are used to select the Enhanced Mini-ACE's clock frequency, as follows:

CLK_SEL_1 | CLK_SEL_0 | Clock Frequency
0 | 0 | 10 MHz
0 | 1 | 20 MHz
1 | 0 | 12 MHz
1 | 1 | 16 MHz</td></tr>
<tr><td>A14</td><td>A14 / CLK_SEL_0</td><td>8</td><td>For BU-61864(5) (64K RAM version), this signal is always configured as address line A14. Refer to the description of A11-A0 below.

For BU-61843(5)/61743(5) (4K RAM version), if UPADDREN is connected to logic "1", this signal operates as A14.

For BU-61843(5)/61743(5) (4K RAM version), if UPADDREN is connected to logic "0", then this signal operates as CLK_SEL_1. In this case, CLK_SEL_1 and CLK_SEL_0 are used to select the Enhanced Mini-ACE's clock frequency, as defined in the description for A15/CLK_SEL1 above.</td></tr>
<tr><td>A13</td><td>A13 / Vcc -LOGIC</td><td>71</td><td>For BU-61864(5) (64K RAM version), this signal is always configured as address line A13. Refer to the description for A11-A0 below.

For BU-61843(5)/61743(5) (4K RAM version), if UPADDREN is connected to logic "1", this signal operates as A13.

For BU-61843(5)/61743(5) (4K RAM version), if UPADDREN is connected to logic "0", then this signal MUST be connected to +5V/+3.3V-LOGIC (logic "1").</td></tr>
<tr><td>A12</td><td>A12 / $\overline{\text{RTBOOT}}$</td><td>70</td><td>For BU-61864(5) (64K RAM version), this signal is always configured as address line A12. Refer to the description for A11-A0 below.

For BU-61843(5)/61743(5) (4K RAM version), if UPADDREN is connected to logic "1", this signal operates as A12.

For BU-61843(5)/61743(5) (4K RAM version), if UPADDREN is connected to logic "0", then this signal functions as $\overline{\text{RTBOOT}}$. If $\overline{\text{RTBOOT}}$ is connected to logic "0", the Enhanced Mini-ACE will initialize in RT mode with the Busy status word bit set following power turn-on. If $\overline{\text{RTBOOT}}$ hard-wired to logic "1", the Enhanced Mini-ACE will initialize in either Idle mode (for an RT-only part), or in BC mode (for a BC/RT/MT part).</td></tr>
</table>

PROCESSOR ADDRESS BUS (CONTINUED)			
SIGNAL NAME		**PIN**	**DESCRIPTION**
BU-61864(5) (64K RAM)	**BU-61843(5) / 61743(5) (4KK RAM)**		
A11	A11	3	Lower 12 bits of 16-bit bi-directional address bus. In both the buffered and transparent modes, the host CPU accesses the Enhanced Mini-ACE registers and internal RAM by means of A11 - A0 (4K version). For the 64K versions, A15 - A12 are also used for this purpose. In buffered mode, A12-A0 (or A15-A0) are inputs only. In the transparent mode, A12-A0 (or A15-A0) are inputs during CPU accesses and become outputs, driving outward (towards the CPU) when the 1553 protocol/memory management logic accesses up to 64K words of external RAM. In transparent mode, the address bus is driven outward only when the signal $\overline{\text{DTACK}}$ is low (indicating that the Enhanced Mini-ACE has control of the RAM interface bus) and IOEN is high, indicating a non-host access. Most of the time, including immediately after power turn-on, A12-A0 (or A15-A0) will be in high impedance (input) state.
A10	A10	4	
A9	A9	69	
A8	A8	6	
A7	A7	11	
A6	A6	22	
A5	A5	68	
A4	A4	9	
A3	A3	10	
A2	A2	12	
A1	A1	27	
A0(LSB)	A0(LSB)	15	

PROCESSOR INTERFACE CONTROL		
SIGNAL NAME	**PIN**	**DESCRIPTION**
$\overline{\text{SELECT}}$ (1)	61	Generally connected to a CPU address decoder output to select the Enhanced Mini-ACE for a transfer to/from either RAM or register.
$\overline{\text{STRBD}}$ (1)	62	Strobe Data. Used in conjunction with $\overline{\text{SELECT}}$ to initiate and control the data transfer cycle between the host processor and the ENHANCED MINI-ACE. $\overline{\text{STRBD}}$ must be asserted low through the full duration of the transfer cycle.
RD / $\overline{\text{WR}}$	63	Read/Write. For a host processor access, RD/$\overline{\text{WR}}$ selects between reading and writing. In the 16-bit buffered mode, if POL_SEL is logic "0, then RD/$\overline{\text{WR}}$ should be low (logic “0") for read accesses and high (logic "1") for write accesses. If POL_SEL is logic "1", or the interface is configured for a mode other than 16-bit buffered mode, then RD/$\overline{\text{WR}}$ is high (logic "1") for read accesses and low (logic "0") for write accesses.
ADDR_LAT(1) / $\overline{\text{MEMOE}}$ (0)	14	Memory Output Enable or Address Latch. In buffered mode, the ADDR_LAT input is used to configure the buffers for A15-A0, $\overline{\text{SELECT}}$, MEM/$\overline{\text{REG}}$, and MSB/LSB (for 8-bit mode only) in latched mode (when low) or transparent mode (when high). That is, the Enhanced Mini-ACE's internal transparent latches will track the values on A15-A0, $\overline{\text{SELECT}}$, MEM/$\overline{\text{REG}}$, and MSB/LSB when ADDR_LAT is high, and latch the values when ADDR_LAT goes low. In general, for interfacing to processors with a non-multiplexed address/data bus, ADDR_LAT should be hardwired to logic "1". For interfacing to processors with a multiplexed address/data bus, ADDR_LAT should be connected to a signal that indicates a valid address when ADDR_LAT is logic "1". In transparent mode, $\overline{\text{MEMOE}}$ output signal is used to enable data outputs for external RAM read cycles (normally connected to the $\overline{\text{OE}}$ input signal on external RAM chips).
$\overline{\text{ZEROWAIT}}$ (1) / $\overline{\text{MEMWR}}$ (0)	23	Memory Write or Zero Wait . In buffered mode, input signal ($\overline{\text{ZEROWAIT}}$) used to select between the zero wait mode ($\overline{\text{ZEROWAIT}}$ = “0") and the non-zero wait mode ($\overline{\text{ZEROWAIT}}$ = "1"). In transparent mode, active low output signal ($\overline{\text{MEMWR}}$) asserted low during memory write transfers to strobe data into external RAM (normally connected to the $\overline{\text{WR}}$ input signal on external RAM chips).
16 / $\overline{8}$ (1) / $\overline{\text{DTREQ}}$ (0)	24	Data Transfer Request or Data Bus Select. In buffered mode, input signal 16/$\overline{8}$ used to select between the 16 bit data transfer mode (16/$\overline{8}$= "1") and the 8-bit data transfer mode (16/$\overline{8}$ = "0"). In transparent mode (16-bit only), active low level output signal $\overline{\text{DTREQ}}$ used to request access to the processor/RAM interface bus (address and data buses).
MSB / LSB (1) / $\overline{\text{DTGRT}}$ (1)	64	Data Transfer Grant or Most Significant Byte/Least Significant Byte. In 8-bit buffered mode, input signal (MSB/LSB) used to indicate which byte is currently being transferred (MSB or LSB). The logic sense of MSB/LSB is controlled by the POL_SEL input. MSB/LSB is not used in the 16-bit buffered mode. In transparent mode, active low input signal ($\overline{\text{DTGRT}}$) asserted in response to the $\overline{\text{DTREQ}}$ output to indicate that control of the external processor/RAM bus has been transferred from the host processor to the Enhanced Mini-ACE.
POL_SEL (1) / $\overline{\text{DTACK}}$ (0)	29	Data Transfer Acknowledge or Polarity Select. In 16-bit buffered mode, if POL_SEL is connected to logic "1", RD/$\overline{\text{WR}}$ should be asserted high (logic "1") for a read operation and low (logic "0") for a write operation. In 16-bit buffered mode, if POL_SEL is connected to logic "0", RD/$\overline{\text{WR}}$ should be asserted low (logic "0") for a read operation and high (logic "1") for a write operation. In 8-bit buffered mode (TRANSPARENT/ $\overline{\text{BUFFERED}}$ = “0" and 16/$\overline{8}$ = "0"), POL_SEL input signal used to control the logic sense of the MSB/$\overline{\text{LSB}}$ signal. If POL_SEL is connected to logic “0", MSB/$\overline{\text{LSB}}$ should be asserted low (logic "0") to indicate the transfer of the least significant byte and high (logic "1") to indicate the transfer of the most significant byte. If POL_SEL is connected to logic “1", MSB/$\overline{\text{LSB}}$ should be asserted high (logic "1") to indicate the transfer of the least significant byte and low (logic "0") to indicate the transfer of the most significant byte. In transparent mode, active low output signal ($\overline{\text{DTACK}}$) used to indicate acceptance of the processor/RAM interface bus in response to a data transfer grant ($\overline{\text{DTGRT}}$). The Enhanced Mini-ACE's RAM transfers over A15-A0 and D15-D0 will be framed by the time that $\overline{\text{DTACK}}$ is asserted low.

PROCESSOR INTERFACE CONTROL		
SIGNAL NAME	**PIN**	**DESCRIPTION**
TRIG_SEL (1) / MEMENA_IN (1)	28	Memory Enable or Trigger Select input. In 8-bit buffered mode, input signal (TRIG-SEL) used to select the order in which byte pairs are transferred to or from the Enhanced MINI-ACE by the host processor. In the 8-bit buffered mode, TRIG_SEL should be asserted high (logic 1) if the byte order for both read operations and write operations is MSB followed by LSB. TRIG_SEL should be asserted low (logic 0) if the byte order for both read operations and write operations is LSB followed by MSB. This signal has no operation in the 16-bit buffered mode (it does not need to be connected). In transparent mode, active low input MEMENA_IN, used as a Chip Select (CS) input to the Enhanced Mini-ACE's internal shared RAM. If only internal RAM is used, should be connected directly to the output of a gate that is OR'ing the DTACK and IOEN output signals.
MEM / REG(1)	1	Memory/Register. Generally connected to either a CPU address line or address decoder output. Selects between memory access (MEM/REG = "1") or register access (MEM/REG = "0").
SSFLAG (1) / EXT_TRIG(1)	32	Subsystem Flag (RT) or External Trigger (BC/Word Monitor) input. In RT mode, if this input is asserted low, the Subsystem Flag bit will be set in the ENHANCED MINI-ACE's RT Status Word. If the SSFLAG input is logic "0" while bit 8 of Configuration Register #1 has been programmed to logic "1" (cleared), the Subsystem Flag RT Status Word bit will become logic "1," but bit 8 of Configuration Register #1, SUBSYSTEM FLAG, will return logic "1" when read. That is, the sense on the SSFLAG input has no effect on the SUBSYSTEM FLAG register bit. In the non-enhanced BC mode, this signal operates as an External Trigger input. In BC mode, if the external BC Start option is enabled (bit 7 of Configuration Register #1), a low to high transition on this input will issue a BC Start command, starting execution of the current BC frame. In the enhanced BC mode, during the execution of a Wait for External Trigger (WTG) instruction, the Enhanced Mini-ACE BC will wait for a low-to-high transition on EXT_TRIG before proceeding to the next instruction. In the Word Monitor mode, if the external trigger is enabled (bit 7 of Configuration Register #1), a low to high transition on this input will initiate a monitor start. This input has no effect in Message Monitor mode.
TRANSPARENT / BUFFERED	55	Used to select between the buffered mode (when strapped to logic “0”) and transparent/DMA mode (when strapped to logic “1") for the host processor interface.
READYD	56	Handshake output to host processor. For a nonzero wait state read access, READYD is asserted at the end of a host transfer cycle to indicate that data is available to be read on D15 through D0 when asserted (low). For a nonzero wait state write cycle, READYD is asserted at the end of the cycle to indicate that data has been transferred to a register or RAM location. For both nonzero wait reads and writes, the host must assert STRBD low until READYD is asserted low. In the (buffered) zero wait state mode, this output is normally logic "0", indicating that the Enhanced Mini-ACE is in a state ready to accept a subsequent host transfer cycle. In zero wait mode, READYD will transition from low to high during (or just after) a host transfer cycle, when the Enhanced Mini-ACE initiates its internal transfer to or from registers or internal RAM. When the Enhanced Mini-ACE completes its internal transfer, READYD returns to logic "0", indicating it is ready for the host to initiate a subsequent transfer cycle.
IOEN(0)	58	I/O Enable. Tri-state control for external address and data buffers. Generally not used in buffered mode. When low, indicates that the Enhanced Mini-ACE is currently performing a **host** access to an internal register, or internal or (for transparent mode) external RAM. In transparent mode, ~~IOEN~~ (low) should be used to enable external address and data bus tri-state buffers.

RT ADDRESS		
SIGNAL NAME	**PIN**	**DESCRIPTION**
RTAD4 (MSB) (1)	35	RT Address inputs. If bit 5 of Configuration Register #6, RT ADDRESS SOURCE, is programmed to logic "0" (default), then the Enhanced Mini-ACE's RT address is provided by means of these 5 input signals. In addition, if RT ADDRESS SOURCE is logic "0", the source of RT address parity is RTADP. There are many methods for using these input signals for designating the Enhanced Mini-ACE's RT address. For details, refer to the description of RT_AD_LAT. If RT ADDRESS SOURCE is programmed to logic "1", then the Enhanced Mini-ACE's source for its RT address and parity is under software control, via data lines D5-D0. In this case, the RTAD4-RTAD0 and RTADP signals are not used.
RTAD3 (1)	34	
RTAD2 (1)	21	
RTAD1 (1)	41	
RTAD0 (LSB) (1)	33	
RTADP (1)	40	Remote Terminal Address Parity. This input signal must provide an odd parity sum with RTAD4-RTAD0 in order for the RT to respond to non-broadcast commands. That is, there must be an **odd** number of logic "1"s from among RTAD-4-RTAD0 and RTADP.
RT_AD_LAT (1)	31	RT Address Latch. Input signal used to control the Enhanced MINI-ACE's internal RT address latch. If RT_AD_LAT is connected to logic "0", then the Enhanced Mini-ACE RT is configured to accept a hardwired (transparent) RT address from RTAD4-RTAD) and RTADP. If RT_AD_LAT is initially logic "0", and then transitions to logic "1", the values presented on RTAD4-RTAD0 and RTADP will be latched internally on the rising edge of RT_AD_LAT. If RT_AD_LAT is connected to logic "1", then the Enhanced Mini-ACE's RT address is latchable under host processor control. In this case, there are two possibilities: (1) If bit 5 of Configuration Register #6, RT ADDRESS SOURCE, is programmed to logic "0" (default), then the source of the RT Address is the RTAD4-RTAD0 and RTADP input signals; (2) If RT ADDRESS SOURCE is programmed to logic "1", then the source of the RT Address is the lower 6 bits of the processor data bus, D5-D1 (for RTAD4-0) and D0 (for RTADP). In **either** of these two cases (with RT_AD_LAT = "1"), the processor will cause the RT address to be latched by: (1) writing bit 15 of Configuration Register #3, ENHANCED MODE, to logic "1"; (2) writing bit 3 of Configuration Register #4, LATCH RT ADDRESS WITH CONFIGURATION REGISTER #5, to logic "1"; and (3) writing to Configuration Register #5. In the case of RT ADDRESS SOURCE = "1", then the values of RT address and RT address parity must be written to the lower 6 bits of Configuration Register #5, via D5-D0. In the case where RT ADDRESS SOURCE = "0", the bit values presented on D5-D0 become "don't care" .

	MISCELLANEOUS		
SIGNAL NAME	**BU-61864(5) (64K RAM)**	**BU-61843(5) / 61743(5) (4KK RAM)**	**DESCRIPTION**
	PIN	**PIN**	
UPADDREN	-	26	**For BU-61864/61865, this pin is +5V-RAM and MUST be connected to +5V.** For BU-61743(5) and 61843(5), this signal is used to control the function of the upper 4 address inputs (A15-A12). For these versions of Enhanced Mini-ACE, if UPADDREN is connected to logic "1", then these four signals operate as address lines A15-A12. For BU-61843(5)/61743(5), if UPADDREN is connected to logic "0", then A15 and A14 function as CLK_SEL_1 and CLK_SEL_0 respectively; A13 **MUST** be connected to Vcc-LOGIC (+5V or +3.3V); and A12 functions as $\overline{\text{RTBOOT}}$.
$\overline{\text{INCMD}}$ (O) / $\overline{\text{MCRST}}$ (O)	25	25	In-command or Mode Code Reset. The function of this pin is controlled by bit 0 of Configuration Register #7, MODE CODE RESET/$\overline{\text{INCMD}}$ SELECT. If this register bit is logic "0" (default), $\overline{\text{INCMD}}$ will be active on this pin. For BC, RT, or Selective Message Monitor modes, $\overline{\text{INCMD}}$ is asserted low whenever a message is being processed by the Enhanced Mini-ACE. In Word Monitor mode, $\overline{\text{INCMD}}$ will be asserted low for as long as the monitor is online. For RT mode, if MODE CODE RESET/$\overline{\text{INCMD}}$ SELECT is programmed to logic "1", $\overline{\text{MCRST}}$ will be active. In this case, $\overline{\text{MCRST}}$ will be asserted low for two clock cycles following receipt of a Reset remote terminal mode command. In BC or Monitor modes, if MODE CODE RESET/$\overline{\text{INCMD}}$ SELECT is logic "1", this signal is inoperative; i.e., in this case, it will always output a value of logic "1".
$\overline{\text{INT}}$ (0)	57	57	Interrupt Request output. If the LEVEL/$\overline{\text{PULSE}}$ interrupt bit (bit 3) of Configuration Register #2 is logic "0", a negative **pulse** of approximately 500ns in width is output on $\overline{\text{INT}}$ to signal an interrupt request. If LEVEL/$\overline{\text{PULSE}}$ is high, a low **level** interrupt request output will be asserted on $\overline{\text{INT}}$. The level interrupt will be cleared (high) after either: (1) The processor writes a value of logic "1" to INTERRUPT RESET, bit 2 of the Start/Reset Register; or (2) If bit 4 of Configuration Register #2, INTERRUPT STATUS AUTO-CLEAR is logic "1", then it will only be necessary to read the Interrupt Status Register (#1 and/or #2) that is requesting an interrupt that has been enabled by the corresponding Interrupt Mask Register. However, for the case where both Interrupt Status Register #1 and Interrupt Status Register #2 have bits set reflecting interrupt events, it will be necessary to read **both** interrupt status registers in order to clear $\overline{\text{INT}}$.
CLOCK_IN (1)	30	30	20 MHz, 16 MHz, 12 MHz, or 10 MHz clock input.
TX_INH_A (1)	59	59	Transmitter inhibit inputs for the Channel A and Channel B MIL-STD-1553 transmitters. For normal operation, these inputs should be connected to logic "0". To force a shutdown of Channel A and/or Channel B, a value of logic "1" should be applied to the respective TX_INH input.
TX_INH_B (1)	60	60	
$\overline{\text{MSTCLR}}$(1)	2	2	Master Clear. Negative true Reset input, normally asserted low following power turn-on. When coming out of a “reset” condition, please note that the rise time of $\overline{\text{MSTCLR}}$ must be less than 10 µS.

		FACTORY TEST
SIGNAL NAME	**PIN**	**DESCRIPTION**
XCVR_TP (ZAP VOLTA)	P1(*)	For factory test only. **Do not connect** for normal operation.
XCVR_TP (READOUTB)	P2(*)	
XCVR_TP (READOUTA)	P3(*)	
XCVR_TP (CLOCK)	P4(*)	
XCVR_TP ($\overline{\text{RESET}}$)	P5(*)	
XCVR_TP (ZAP VOLTB)	P6(*)	

(*) Note that the Test Output pins are recessed pads located on the bottom of the package.

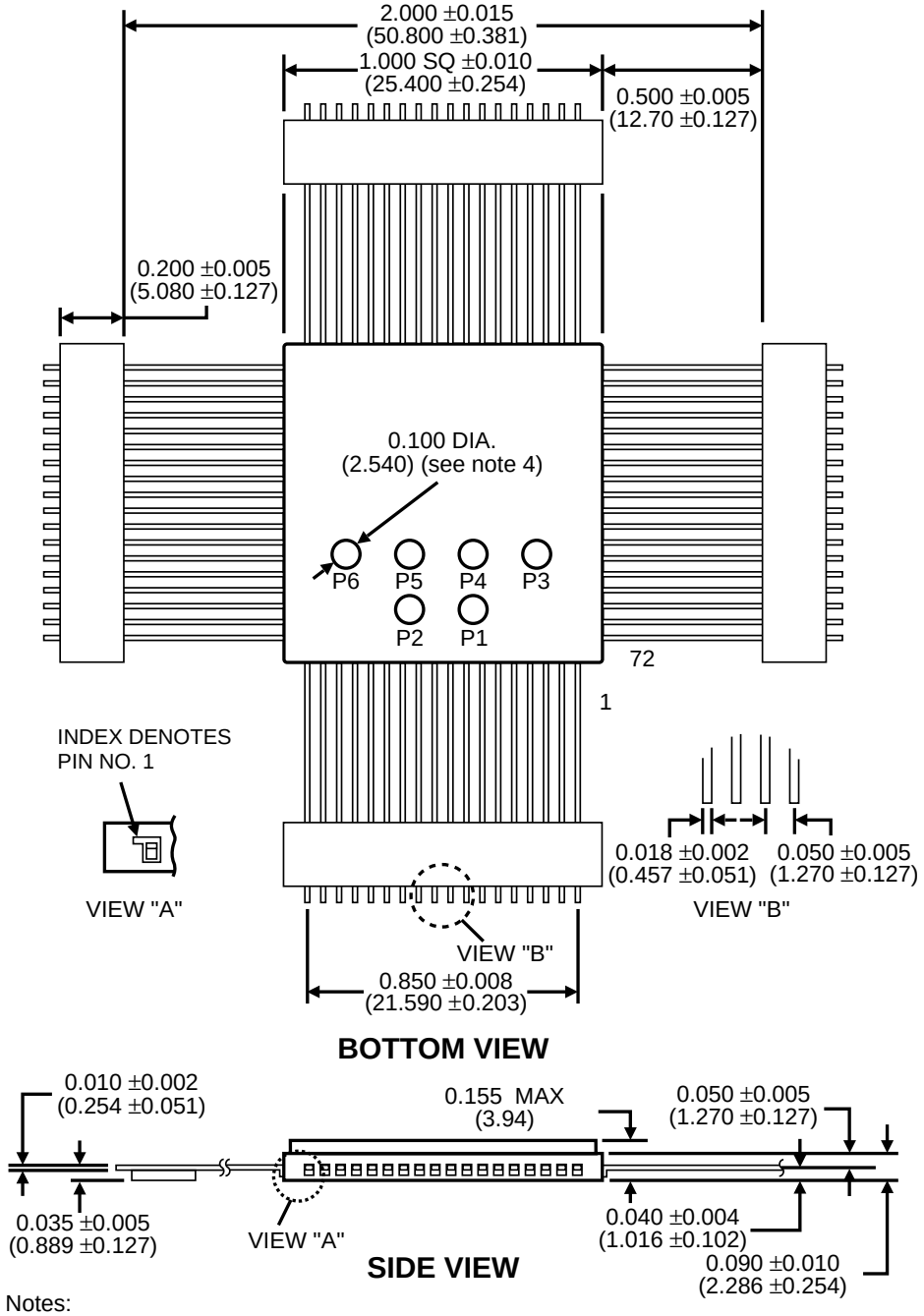
TABLE 48. PACKAGE PINOUTS			
PACKAGE		BU-61864(5) BC / RT / MT (64K RAM)	BU-61843(5) BC / RT / MT, (4K RAM) BU-61743(5) RT ONLY, (4K RAM)
QFP	PGA (NOTE 1)		
1	B4	MEM/$\overline{\text{REG}}$	MEM/$\overline{\text{REG}}$
2	B5	$\overline{\text{MSTCLR}}$	$\overline{\text{MSTCLR}}$
3	C2	A11	A11
4	C3	A10	A10
5	C1	TX/RX_A	TX/RX_A
6	D2	A8	A8
7	D1	$\overline{\text{TX/RX\_A}}$	$\overline{\text{TX/RX\_A}}$
8	C4	A14	A14/CLK_SEL_0
9	E3	A4	A4
10	F2	A3	A3
11	E1	A7	A7
12	F3	A2	A2
13	G1	TX/RX_B	TX/RX_B
14	G4	$\overline{\text{ADDR\_LAT/MEMOE}}$	$\overline{\text{ADDR\_LAT/MEMOE}}$
15	G3	A0	A0
16	H1	$\overline{\text{TX/RX-B}}$	$\overline{\text{TX/RX-B}}$
17	A7	LOGIC GND	LOGIC GND
18	A8	LOGIC GND	LOGIC GND
19	J8	LOGIC GND	LOGIC GND
20	A9	+5V Vcc-CH. B	+5V Vcc-CH. B
21	J7	RTAD2	RTAD2
22	F1	A6	A6
23	J2	$\overline{\text{ZEROWAIT}}$/$\overline{\text{MEMWR}}$	$\overline{\text{ZEROWAIT}}$/$\overline{\text{MEMWR}}$
24	H5	$\overline{8}$/16-BIT/$\overline{\text{DTREQ}}$	$\overline{8}$/16-BIT/$\overline{\text{DTREQ}}$
25	H3	$\overline{\text{INCMD}}$/$\overline{\text{MCRST}}$	$\overline{\text{INCMD}}$/$\overline{\text{MCRST}}$
26	H4	+5V RAM	UPADDREN
27	G2	A1	A1
28	J5	TRIG_SEL/$\overline{\text{MEMENA\_IN}}$	TRIG_SEL/$\overline{\text{MEMENA\_IN}}$
29	J6	POL_SEL/$\overline{\text{DTACK}}$	POL_SEL/$\overline{\text{DTACK}}$
30	H6	CLOCK_IN	CLOCK_IN
31	G7	RT_AD_LAT	RT_AD_LAT
32	H2	$\overline{\text{SSFLAG}}$/ EXT_TRIG	$\overline{\text{SSFLAG}}$/ EXT_TRIG
33	H7	RTAD0	RTAD0
34	G8	RTAD3	RTAD3
35	H8	RTAD4	RTAD4
36	E8	D6	D6
37	D3	+5V/3.3V LOGIC	+5V/3.3V LOGIC

TABLE 48. PACKAGE PINOUTS			
PACKAGE		BU-61864(5) BC / RT / MT (64K RAM)	BU-61843(5) BC / RT / MT, (4K RAM) BU-61743(5) RT ONLY, (4K RAM)
QFP	PGA (NOTE 1)		
38	F8	D1	D1
39	G6	D4	D4
40	G9	RTADP	RTADP
41	J9	RTAD1	RTAD1
42	H9	DO	DO
43	F9	D2	D2
44	F7	D3	D3
45	G5	D5	D5
46	E7	D8	D8
47	E9	D7	D7
48	D7	D13	D13
49	B2	D12	D12
50	D9	D14	D14
51	B9	D9	D9
52	A2	D11	D11
53	D8	D15	D15
54	A1	D10	D10
55	C9	TRANSPARENT/ $\overline{\text{BUFFERED}}$	TRANSPARENT/ $\overline{\text{BUFFERED}}$
56	B8	$\overline{\text{READYD}}$	$\overline{\text{READYD}}$
57	C8	$\overline{\text{INT}}$	$\overline{\text{INT}}$
58	A3	$\overline{\text{IOEN}}$	$\overline{\text{IOEN}}$
59	B7	TX_INH_A	TX_INH_A
60	C7	TX_INH_B	TX_INH_B
61	C6	$\overline{\text{SELECT}}$	$\overline{\text{SELECT}}$
62	A6	$\overline{\text{STRBD}}$	$\overline{\text{STRBD}}$
63	A5	RD / $\overline{\text{WR}}$	RD / $\overline{\text{WR}}$
64	J1	MSB/LSB/$\overline{\text{DTGRT}}$	MSB/LSB/$\overline{\text{DTGRT}}$
65	A4	LOGIC GND	LOGIC GND
66	C5	A15	A15/CLK_SEL_1
67	B6	LOGIC GND	LOGIC GND
68	E2	A5	A5
69	J4	A9	A9
70	B3	A12	A12/$\overline{\text{RTBOOT}}$
71	B1	A13	A13/+5V/3.3V LOGIC
72	J3	+5V Vcc-CH. A	+5V Vcc-CH. A

TABLE 48. PACKAGE PINOUTS			
PACKAGE		BU-61864(5) BC / RT / MT (64K RAM)	BU-61843(5) BC / RT / MT, (4K RAM) BU-61743(5) RT ONLY, (4K RAM)
QFP	PGA (NOTE 1)		
P1 **	D4	XCVR TP (ZAP VOLTA)	XCVR TP (ZAP VOLTA)
P2 **	F5	XCVR TP (READOUTB)	XCVR TP (READOUTB)
P3 **	D5	XCVR TP (READOUTA)	XCVR TP (READOUTA)
P4 **	E4	XCVR TP(CLOCK)	XCVR TP(CLOCK)
P5 **	E5	XCVR TP (RESET_L)	XCVR TP (RESET_L)
P6 **	F4	XCVR TP (ZAP VOLTB)	XCVR TP (ZAP VOLTB)
N/A	D6	GND	GND
N/A	E6	GND	GND
N/A	F6	GND	GND

** Note that the Test Output pins on the flat pack are pads located on the bottom of the package.

NOTE 1: This column is shown for reference only. There is no PGA package for the initial product release.



Notes:
1) Dimensions are in inches (mm).
2) Package Material: Alumina (AL_2O_3)
3) Lead Material: Kovar, Plated by 50µ in. minimum nickel under 60µ in. minimum gold.
4) There are 6 test pads located on the bottom of the package. These pads are recessed so as not to interfere when mounting the hybrid There are no user connections to these pads.

FIGURE 16. MECHANICAL OUTLINE DRAWING FOR 72-LEAD FLATPACK

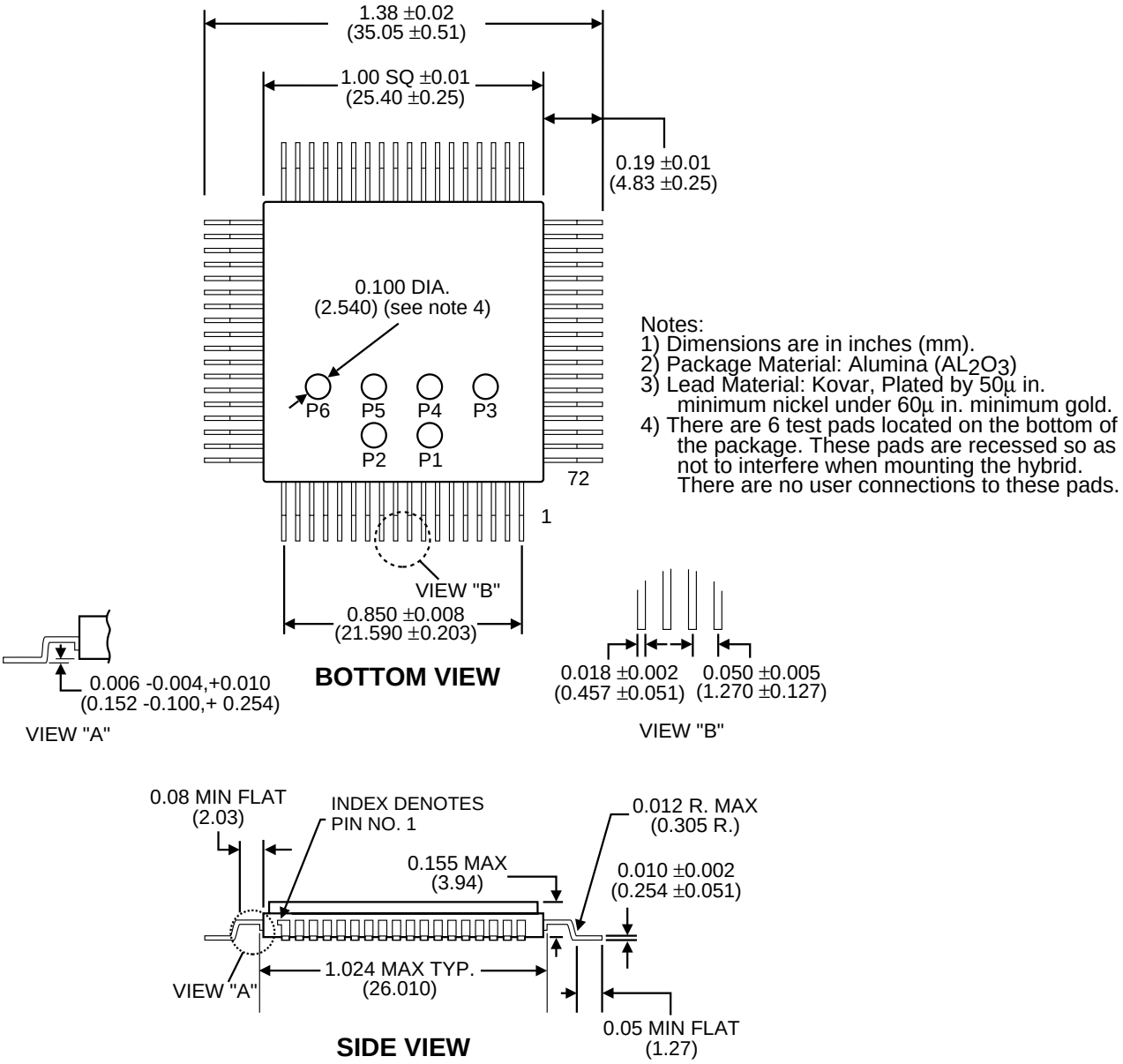


FIGURE 17. MECHANICAL OUTLINE DRAWING FOR 72-PIN GULL LEAD PACKAGE

ORDERING INFORMATION

BU-61745F3-120X

Supplemental Process Requirements:
- S = Pre-Cap Source Inspection
- L = Pull Test
- Q = Pull Test and Pre-Cap Inspection
- K = One Lot Date Code
- W = One Lot Date Code and PreCap Source
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, PreCap Source and 100% Pull Test
- Blank = None of the Above

Test Criteria:
- 0 = Standard Testing
- 2 = MIL-STD-1760 Amplitude Compliant

Process Requirements:
- 0 = Standard DDC practices, no Burn-In
- 1 = MIL-PRF-38534 Compliant
- 2 = B*
- 3 = MIL-PRF-38534 Compliant with PIND Testing
- 4 = MIL-PRF-38534 Compliant with Solder Dip
- 5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip
- 6 = B* with PIND Testing
- 7 = B* with Solder Dip
- 8 = B* with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In

Temperature Range/Data Requirements:
- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 6 = Custom Part (Reserved)
- 7 = Custom Part (Reserved)
- 8 = 0°C to +70°C with Variables Test Data

Voltage/Transceiver Option:
- 3 = +5 Volts rise/fall times = 100 to 300 ns (-1553B)
- 4 = +5 Volts rise/fall times = 200 to 300 ns (-1553B and McAir compatible)

Package Type:
- F = Flat Pack
- G = “Gull Wing” (Formed Lead)

Logic / RAM Voltage
- 3 = 3.3 Volt (Applicable only for BU-61743 and BU-61843)
- 4 = 3.3 and 5 Volt (Applicable only for BU-61684)
- 5 = 5 Volt

Product Type:
- BU-6174 = RT only with 4K x 16 RAM
- BU-6184 = BC /RT / MT with 4K x 16 RAM
- BU-6186 = BC /RT / MT with 64K x 17 RAM

STANDARD DDC PROCESSING		
TEST	**MIL-STD-883**	
	METHOD(S)	**CONDITION(S)**
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	A
BURN-IN	1015, Table 1	—

NOTES

NOTES

105 Wilbur Place, Bohemia, New York 11716-2482

For Technical Support - 1-800-DDC-5757 ext. 7382 or 7234

Headquarters - Tel: (631) 567-5600, Fax: (631) 567-7358
West Coast - Tel: (714) 895-9777, Fax: (714) 895-4988
Southeast - Tel: (703) 450-7900, Fax: (703) 450-6610
United Kingdom - Tel: +44-(0)1635-811140, Fax: +44-(0)1635-32264
Ireland - Tel: +353-21-341065, Fax: +353-21-341568
France - Tel: +33-(0)1-41-16-3424, Fax: +33-(0)1-41-16-3425
Germany - Tel: +49-(0)8141-349-087, Fax: +49-(0)8141-349-089
Sweden - Tel: +46-(0)8-54490044, Fax +46-(0)8-7550570
Japan - Tel: +81-(0)3-3814-7688, Fax: +81-(0)3-3814-7689
World Wide Web - http://www.ddc-web.com

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